# M. Tech.

IN

# VLSI SYSTEM

# CURRICULUM

## (For students admitted in 2019-2021)

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**
**NATIONAL INSTITUTE OF TECHNOLOGY**
**TIRUCHIRAPPALLI – 620 015**
**TAMIL NADU, INDIA**

## Institute Vision and Mission

**Vision**

- To be a university globally trusted for technical excellence where learning and research integrate to sustain society and industry.

**Mission**

- To offer undergraduate, postgraduate, doctoral and modular programmes in multi-disciplinary / inter-disciplinary and emerging areas.
- To create a converging learning environment to serve a dynamically evolving society.
- To promote innovation for sustainable solutions by forging global collaborations with academia and industry in cutting-edge research.
- To be an intellectual ecosystem where human capabilities can develop holistically.

## Department Vision and Mission

**Vision**

- To excel in education and research in Electronics and Communication Engineering

**Mission**

- To educate with the state of art technologies to meet the growing challenges of the industry.
- To carry out research through constant interaction with research organizations and industry.
- To equip the students with strong foundations to enable them for continuing Education.

## Program Educational Objectives (PEOs)

- **PEO1:** Graduates will be successful in facing the challenges in their professional career in industry, government and academia by integrating the existing and advanced knowledge in VLSI Systems to solve complex problems in Electronics and Communication engineering.

- **PEO2:** Graduates will be efficient in adapting new technologies, achieve excellence in their professional career, lead research as well as development projects/activities and establish themselves as successful professional.

- **PEO3:** Graduates will practice and inspire high ethical and technical standards, possess technical competency in VLSI Systems and take up higher studies.

## Program Outcomes (POs)

- **PO1:** To acquire in-depth knowledge in Embedded System, Digital VLSI and Mixed Signal Systems including wider and global perspective, with an ability to discriminate, evaluate, analyse and synthesise existing and new knowledge, and integration of the same for enhancement of knowledge.

- **PO2:** To design and analyse complex VLSI/Embedded circuits critically, using appropriate analytical methods as well as front end and back end tools including prediction and modelling at industry standards with an understanding of the limitations.

- **PO3:** An ability to independently carry out research /investigation and development work to solve practical problems and have the preparedness for lifelong learning.

- **PO4:** To comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

- **PO5:** Students should be able to demonstrate a degree of mastery in VLSI/Embedded system by way of developing new algorithms, techniques, solutions to domestic and industrial problems.

- **PO6:** To acquire professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society

## CURRICULUM

The total minimum credits for completing the M.Tech. Programme in VLSI System is 66.

### SEMESTER I

| Sl. No. | Course Code | Course of | Credits |
|---|---|---|---|
| 1. | MA617 | Graph Theory and Discrete Optimization | 3 |
| 2. | EC651 | Analog VLSI | 3 |
| 3. | EC653 | Basics of VLSI | 3 |
| 4. | | Elective I | 3 |
| 5. | | Elective II | 3 |
| 6. | | Elective III | 3 |
| 7. | EC655 | HDL Programming Laboratory | 2 |
| **Total** | | | **20** |

### SEMESTER II

| Sl. No. | Course Code | Course Title | Credits |
|---|---|---|---|
| 1. | EC652 | VLSI System Testing | 3 |
| 2. | EC654 | Electronic Design Automation Tools | 3 |
| 3. | EC656 | Design of ASICs | 3 |
| 4. | | Elective IV | 3 |
| 5. | | Elective V | 3 |
| 6. | | Elective VI | 3 |
| 7. | EC658 | Analog IC Design Laboratory | 2 |
| 8. | EC660 | ASIC – CAD Laboratory | 2 |
| **Total** | | | **22** |

## SEMESTER III

| Course Code | Course Title | Credits |
|---|---|---|
| EC697 | PROJECT WORK - PHASE I | 12 |
| **Total** | | **12** |

## SEMESTER IV

| Course Code | Course Title | Credits |
|---|---|---|
| EC698 | PROJECT WORK - PHASE II | 12 |
| **Total** | | **12** |

## LIST OF ELECTIVES

| Sl. No. | Course Code | Course Title | Credits |
|---|---|---|---|
| 1. | EC661 | Digital System Design | 3 |
| 2. | EC662 | Modelling and Synthesis with Verilog HDL | 3 |
| 3. | EC663 | Optimization of Digital Signal Processing structures for VLSI | 3 |
| 4. | EC664 | Cognitive Radio | 3 |
| 5. | EC665 | VLSI Process Technology | 3 |
| 6. | EC666 | Analysis and Design of Digital Systems using VHDL | 3 |
| 7. | EC667 | Advanced Computer Architecture | 3 |
| 8. | EC668 | Low Power VLSI Systems | 3 |
| 9. | EC669 | VLSI Digital Signal Processing Systems | 3 |
| 10. | EC670 | Asynchronous System Design | 3 |
| 11. | EC671 | Advanced Digital Design | 3 |
| 12. | EC672 | Physical Design Automation | 3 |
| 13. | EC673 | Mixed - Signal Circuit Design | 3 |
| 14. | EC674 | RF circuits | 3 |

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|---|---|---|---|
| 15. | EC675 | Functional Verification using Hardware Verification Languages | 3 |
| 16. | EC676 | Testability of Analog / Mixed-Signal Circuits and<br>High Speed Circuit Design | 3 |
| 17. | EC677 | High Speed System Design | 3 |
| 18. | EC678 | Modelling of Solid-State Devices | 3 |
| 19. | EC679 | Nano-Scale Devices: Modelling and Circuits | 3 |
| 20. | EC680 | Embedded System Design | 3 |
| 21. | EC681 | Internet of Things | 3 |
| 22. | EC682 | Design and Testing of Advanced Semiconductor Memories | 3 |
| 23. | EC683 | FPGA Based System Design | 3 |
| 24. | EC684 | Bio-Medical CMOS ICs | 3 |
| 25. | EC685 | On-chip Antenna Design | 3 |
| 26. | EC612 | DSP Architecture | 3 |
| 27. | EC613 | High Speed Communication Networks | 3 |
| 28. | EC615 | Digital Image Processing | 3 |
| 29. | EC616 | RF MEMS | 3 |
| 30. | EC626 | Bio MEMS | 3 |

## LIST OF OPEN ELECTIVES

| Sl. No. | Course Code | Course Title | Credits |
|---|---|---|---|
| 1. | MA617 | Graph Theory and Discrete Optimization | 3 |
| 2. | EC653 | Basics of VLSI | 3 |
| 3. | EC662 | Modelling and Synthesis with Verilog HDL | 3 |
| 4. | EC668 | Low Power VLSI Systems | 3 |

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|---|---|---|
| **Course Code** | **:** | **MA617** |
| **Course Title** | **:** | **Graph Theory and Discrete Optimization** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Core** |

**Course Learning Objective**

- To have general awareness of some application oriented concepts in discrete structures and apply them as a tool in the problems related to general communication network.

**Course Content**

Basic definitions, examples and some results, relating degree, walk, trail, path, tour, cycle, complement of a graph, self-complementary graph, Connectedness, Connectivity, distance, shortest path, radius, diameter and Bipartite graphs. Some eccentric properties of graphs, tree, spanning tree, coding of spanning tree. Number of spanning trees in a complete graph. Recursive procedure to find number of spanning trees. Construction of spanning trees.

Directed graphs: some standard definitions and examples of strongly, weakly, unilaterally connected digraphs, strong components and deadlock. Matrix representation of graph and digraphs. Some properties (proof not expected). Eulerian graphs and standard results relating to characterization of Eulerian graphs. Hamiltonian graph-standard theorems (Dirac theorem, Chavtal theorem, closure of graph). Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems.

Chromatic number; vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity, Five colour theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.

Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs.

DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.

**Text Books**

1. *J.A. Bondy and U.S.R.Murthy, "Graph Theory with Applications", Macmillan, London, 1976, EBook, Freely Downloadable.*
2. *Cormen, Leiserson, Rivest and Stein, "Introduction to Algorithms", 2nd Edition, McGraw-Hill, 2001.*

**Reference Books**

1. *M.Gondran and M.Minoux, "Graphs and Algorithms", John Wiley, 1984.*
2. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*

**Course outcomes**

At the end of the course student will be able to

CO1: understand the various types of graphs, graph properties and give examples for the given property
CO2: model the given problem from their field to underlying graph model.
CO3: proceed to solve the problem either through approximation algorithm or exact algorithm depending on the problem nature.
CO4: appreciate the applications of digraphs and graphs in various communication networks.
CO5: appreciate the applications of graphs and digraphs in various other fields.

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|---|---|---|
| **Course Code** | **:** | **EC651** |
| **Course Title** | **:** | **Analog VLSI** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Core** |

**Course Learning Objectives**

- To develop the ability to design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.
- To develop the skills to design analog VLSI circuits for a given specification.

**Course Content**

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.

Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch.

**Text Books**

1. *B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition 2016.*
2. *Paul. R.Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.*

**Reference Books**

1. *T. C. Carusone, D. A. Johns and K. Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.*
2. *P.E.Allen and D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.*
3. *R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.*
4. *Recent literature in Analog IC Design.*

**Course outcomes**

At the end of the course student will be able to
CO1: draw the equivalent circuits of MOS based Analog VLSI and analyse their performance.
CO2: design analog VLSI circuits for a given specification.
CO3: analyse the frequency response of the different configurations of an amplifier.
CO4: understand the feedback topologies involved in the amplifier design.
CO5: appreciate the design features of the differential amplifiers.

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|---|---|---|
| **Course Code** | **:** | **EC653** |
| **Course Title** | **:** | **Basics of VLSI** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Core** |

**Course Learning Objectives**

- To provide rigorous foundation in MOS and CMOS digital circuits
- To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity

**Course Content**

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops, CMOS fabrication and layout, VLSI design flow.

MOS transistor theory: Ideal I-V and C-V characteristics, non-ideal I-V effects, DC transfer characteristics, Switch level RC delay models.

CMOS technologies: Layout design rules, CMOS process enhancement, Technology related CAD issues.

Circuit characterization and performance estimation: Delay estimation, Logical effort and transistor sizing, Power dissipation, Interconnect design margin, Reliability, Scaling.

Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits.

**Text Books**

1. *N.H.E.Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4$^{th}$ Edition, Pearson, 2011.*
2. *J.Rabey and B. Nikolic, "Digital Integrated circuits", 2$^{nd}$ Edition, Pearson, 2003.*

**Reference Books**

1. *Pucknell and Eshraghian, "Basic VLSI Design", 3$^{rd}$ Edition, PHI, 1996.*
2. *Recent literature in Basics of VLSI.*

**Course outcomes**

At the end of the course student will be able to
CO1: implement the logic circuits using MOS and CMOS technology.
CO2: analyse various circuit configurations and their applications
CO3: analyse the merits of circuits according to the technology and applications change.
CO4: design low power CMOS VLSI circuits.
CO5: understand the rapid advances in CMOS Technology

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|---|---|---|
| **Course Code** | **:** | **EC655** |
| **Course Title** | **:** | **HDL Programming Laboratory** |
| **Number of Credits** | **:** | **2** |
| **Course Type** | **:** | **Laboratory** |

**List of Experiments**

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flip flop
6. Shift Register/ Universal Shift Register
7. Comparator
8. Up counter/ Down counter
9. Udps
10. Memory – ROM, RAM
11. Array Multiplier/ Array Multiplier With Pipelining
12. Fir Filter/ Fir Filter With Pipelining

**List of Experiments**

1. Design of 8-bit Carry Skip Adder and Carry Save Adder
2. Design of 4-bit Array Multiplier with and without Pipelining
3. Design of 4-tap FIR Filter with and without Pipelining
4. Design of FIFO
5. Design of Sequence Detector
6. Design of 8-bit ALU
7. Project: Design of 16-point FFT

**Course outcomes:**

After successful completion of the laboratory course, the students are able to

CO1: to learn the basic HDL functions

CO2: Design and analyse the combinational and sequential circuits using Verilog HDL tools.

CO3: Perform FPGA Implementation for Verilog HDL designs on development board

CO4: Implement FIR algorithms in FPGA

CO5: Implement FFT algorithm in FPGA

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|---|---|---|
| **Course Code** | **:** | **EC652** |
| **Course Title** | **:** | **VLSI System Testing** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Core** |

**Course Learning Objective**

- To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

**Course Content**

Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

**Text Books**

1. *N. Jha and S.D. Gupta, "Testing of Digital Systems", Cambridge, 2003.*
2. *W. W. Wen, "VLSI Test Principles and Architectures Design for Testability", Morgan Kaufmann Publishers. 2006.*

**Reference Books**

1. *Michael L. Bushnell and Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory and Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.*
2. *P. K. Lala, "Digital circuit Testing and Testability", Academic Press. 1997.*
3. *M. Abramovici, M. A. Breuer, and A.D. Friedman, "Digital System Testing and Testable Design", Computer Science Press, 1990.*
4. *Recent literature in VLSI System Testing.*

**Course outcomes**

At the end of the course student will be able to

CO1: apply the concepts in testing which can help them design a better yield in IC design.
CO2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
CO3: analyse the various test generation methods for static and dynamic CMOS circuits.
CO4: identify the design for testability methods for combinational and sequential CMOS circuits.
CO5: recognize the BIST techniques for improving testability.

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|---|---|---|
| **Course Code** | **:** | **EC654** |
| **Course Title** | **:** | **Electronic Design Automation Tools** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Core** |

**Course Learning Objective**

- To make the students exposed to Front end and Back end VLSI CAD tools.

**Course Content**

OS Architecture: System settings and configuration. Introduction to UNIX commandsHandling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection. Working on Vi editor, Basic Shell Programming, TCL Scripting language.

Circuit simulation using Spice - circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and Opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

Synthesis and simulation using HDLs-Logic synthesis using Verilog. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

System Verilog- Introduction, Design hierarchy, Data types, Operators and language constructs. Functional coverage, Assertions, Interfaces and test bench structures.
Analog/Mixed Signal Modelling and Verification: Analog/Mixed signal modelling using Verilog-A and Verilog-AMS. Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling using Verilog-RNM/System Verilog. Analog/Digital Boundary Issues: boundary issues coverage. Introduction to Universal Verification Methodology (UVM).

**Text Books**

1. *M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2008.*
2. *M.H.Rashid, "Spice for Circuits and Electronics using Pspice", 2nd Edition, PHI.*
3. *S.Sutherland, S. Davidmann and P. Flake, "System Verilog for Design", 2nd Edition, Springer, 2006.*

**Reference Books**

1. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*
2. *Z. Dr Mark, "Digital System Design with System Verilog", Pearson, 2010.*
3. *Sharon Rosenberg and Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", 2nd edition, 2010.*

**Course outcomes**

After successful completion of the course the students are able to
CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script
CO2: write Pspice code for any electronics circuit and to perform monte-carlo analysis and sensitivity/worst case analysis.
CO3: design synthesizable Verilog and VHDL code.
CO4: explain the difference between Verilog and system Verilog and are able to write system Verilog code.
CO5: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS.

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|---|---|---|
| **Course Code** | **:** | **EC656** |
| **Course Title** | **:** | **Design of ASICs** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Core** |

**Course Learning Objectives**

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and Platform based design.
- To give the student an understanding of High performance algorithms.

**Course Content**

Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs – Anti-fuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors. Self-Study: Multi-core processors, High performance computing (HPC), Cache, High speed memories (DDR4), High speed serdes (56Gbps, PAM4), GPU, High performance algorithms for ASICs/ SoCs, FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs.

ASIC physical design issues, System Partitioning, Floor planning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs and Applications. Schematic and layout basics, Full Custom Design Flow.

Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.

Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM. System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. **Case study:** FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs(I2C, PWM, GPIO, SPI, NAND, Ethernet, USB, high speed serdes etc. are interconnected through AXI/APB buses (protocols and interconnects)

**Text Books**


1. *M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2003.*
2. *Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier, 2008.*


**Reference Books**


1. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*
2. *Jan.M.Rabaey et al, "Digital Integrated Circuit Design Perspective", 2nd Edition, PHI 2003.*
3. *David A.Hodges, "Analysis and Design of Digital Integrated Circuits", 3rd Edition, MGH 2004.*
4. *Hoi-Jun Yoo, Kangmin Lee and Jun Kyong Kim, "Low-Power NoC for High-Performance SoC Design", CRC Press, 2008.*
5. *"An Integrated Formal Verification solution DSM sign-off market trends", www.cadence.com.*

6. *Recent literature in Design of ASICs.*

**Course outcomes**

At the end of the course student will be able to

CO1: explain VLSI tool-flow and appreciate FPGA architecture.

CO2: describe the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.

CO3: explain the algorithms used for ASIC construction

CO4: analyse the basics of System on Chip, On chip communication architectures like AMBA,AXI and utilizing Platform based design.

CO5: synthesize high performance algorithms available for ASICs

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|---|---|---|
| **Course Code** | **:** | **EC658** |
| **Course Title** | **:** | **Analog IC Design Laboratory** |
| **Number of Credits** | **:** | **2** |
| **Course Type** | **:** | **Laboratory** |

**List of Experiments**

1. Characteristics of NMOS and PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Common Gate Amplifier
4. Design of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Opamp
9. Design of Telescopic Cascode Opamp
10. Design of Folded Cascode Opamp

**Course outcomes**

After successful completion of the laboratory course, the students are able to

CO1: Introduce industry standard Analog IC design EDA tool

CO2: Practical learning and understanding of Analog amplifiers, current mirrors etc.

CO3: Solve analog design problems by changing the design parameter of the circuit with the help of Cadence Virtuoso.

CO4: understand the working of circuits and enhance the analog design skills.

CO5: Learn the art of analog layout in IC design.

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|---|---|---|
| **Course Code** | **:** | **EC 660** |
| **Course Title** | **:** | **ASIC – CAD Laboratory** |
| **Number of Credits** | **:** | **2** |
| **Course Type** | **:** | **Laboratory** |

**List of Experiments**

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. MAC
7. Memory

The above experiments are carried out using the following tools:

1. Model SIM
2. Cadence
3. Synopsis
4. Mentor Graphics
5. Xilinx Plan ahead

**List of Experiments**

1. Design of MOD 10 Counter using Verilog
2. Design of MAC Unit using Verilog
3. Design of 8 bit Signed Booth Multiplier using Verilog
4. Design of 4 tap FIR Filter using Verilog
5. Design of Address Generator block for WiMAX Interleaver using Verilog
6. Project: Design of Vending Machine Block using Verilog

The above experiments are carried out using the following tools:

1. Xilinx ISE Design Suite
2. Cadence
3. Synopsis

**Course outcomes:**

After successful completion of the laboratory course, the students are

CO1: Familiar with sophisticated VLSI CAD tools available in the lab.

CO2: Able to design and implement any ASIC designs using the latest VLSI CAD tools.

CO3: Perform full custom ASIC design of digital blocks

CO4: Learn advanced features in physical design

CO5: Complete cycle from design to chip tape-out procedure

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|---|---|---|
| **Course Code** | **:** | **EC661** |
| **Course Title** | **:** | **Digital System Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To get an idea about designing complex, high speed digital systems and how to implement such design.

**Course Content**

Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.

Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures- Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

**Text Books**

1. *N.H.E.Weste, D. Harris, "CMOS VLSI Design, 4th Edition", Pearson, 2010.*
2. *W.Wolf, "FPGA- based System Design", Pearson, 2004.*
3. *S.Hauck and A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008.*

**Reference Books**

1. *F.P. Prosser and D. E. Winkel, "Art of Digital Design", 1987.*
2. *R.F.Tinde, "Engineering Digital Design", 2nd Edition, Academic Press, 2000.*
3. *C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.*
4. *M.Gokhale and P.S.Graham, "Reconfigurable computing: accelerating computation with field-programmable gate arrays", Springer, 2005.*
5. *C.Roth, "Fundamentals of Digital Logic Design", Jaico Publishers, 5th Edition, 2009.*
6. *Recent literature in Digital System Design.*

**Course outcomes**

At the end of the course student will be able to

CO1: identify mapping algorithms into architectures.
CO2: summarize various delays in combinational circuit and its optimization methods.
CO3: summarize circuit design of latches and flip-flops.
CO4: construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
CO5: summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.

| | | |
|---|---|---|
| **Course Code** | **:** | **EC662** |
| **Course Title** | **:** | **Modeling and Synthesis with Verilog HDL** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioural and RTL modelling of digital circuits
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools
- To simulate, synthesize, and program their designs on a development board
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

**Course Content**

Hardware modelling with the verilog HDL. Encapsulation, modelling primitives, different types of description.
Logic system, data types and operators for modelling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.
Behavioural descriptions in verilog HDL. Synthesis of combinational logic.

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

**Text Books**

1. *M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PHI, 1999.*
2. *S. Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson, 2003.*

**Reference Books**

1. *J Bhaskar, "A Verilog HDL Primer", 3rd Edition, Kluwer, 2005.*
2. *M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.*
3. *Recent literature in Modeling and Synthesis with Verilog HDL.*

**Course outcomes**

At the end of the course student will be able to
CO1: understand the basic concepts of verilog HDL
CO2: model digital systems in verilog HDL at different levels of abstraction
CO3: know the simulation techniques and test bench creation.
CO4: understand the design flow from simulation to synthesizable version
CO5: get an idea of the process of synthesis and post-synthesis

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|---|---|---|
| **Course Code** | **:** | **EC663** |
| **Course Title** | **:** | **Optimizations of Digital Signal Processing Structures for VLSI** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To enable students to design VLSI system with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

**Course Content**

An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.

Transformation Techniques: Iteration bound, Retiming, Folding and Unfolding
Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems, Asynchronous pipelining.

**Text Book**

1. *K.K.Parhi, "VLSI Digital Signal Processing Systems: Design And Implementation", John-Wiley, 2010.*

**Reference Books**

1. *U. Meyer -Baese, "Digital Signal Processing with FPGAs", Springer, 2014*
2. *Wayne Burleson, Konstantinos Konstantinides, Teresa H. Meng, "VLSI Signal Processing", 1996.*
3. *Richard J. Higgins, "Digital signal processing in VLSI", 1990.*
4. *Sun Yuan Kung, Harper J. Whitehouse, "VLSI and modern signal processing", 1985*
5. *Magdy A. Bayoumi, "VLSI Design Methodologies for Digital Signal Processing", 2012*
6. *Earl E. Swartzlander, "VLSI signal processing systems", 1986.*
7. Recent literature in *Optimizations of Digital Signal Processing Structures for VLSI.*

**Course outcomes**

At the end of the course student will be able to
CO1: understand the overview of DSP concepts and design architectures for DSP algorithms.
CO2: improve the overall performance of DSP system through various transformation and optimization techniques.
CO3: perform pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.
CO4: optimize design in terms of computation complexity and speed.
CO5: understand clock based issues and design asynchronous and wave pipelined systems.

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| **Course Code** | **:** | **EC664** |
| **Course Title** | **:** | **Cognitive Radio** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- This subject introduces the fundamentals of multi rate signal processing and cognitive radio.

**Course Content**

Filter banks-uniform filter bank. Direct and DFT approaches. Introduction to ADSL Modem. Discrete multi-tone modulation and its realization using DFT. QMF. STFT. Computation of DWT using filter banks.

DDFS- ROM LUT approach. Spurious signals, jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC.CORDIC architectures.

Block diagram of a software radio. Digital down converters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS. Down conversion using discrete Hilbert transform. Under sampling receivers, Coherent demodulation schemes.

Concept of Cognitive Radio, Benefits of Using SDR, Problems Faced by SDR, Cognitive Networks, Cognitive Radio Architecture. Cognitive Radio Design, Cognitive Engine Design.

A Basic OFDM System Model, OFDM based cognitive radio, Cognitive OFDM Systems, MIMO channel estimation, Multi-band OFDM, MIMO-OFDM synchronization and frequency offset estimation. Spectrum sensing to detect Specific Primary System, Spectrum Sensing for Cognitive OFDMA Systems.

**Text Books**

1. *U. Meyer – Baese, "Digital Signal Processing with FPGAs", Springer, 2004.*
2. *H. Arslan "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", University of South Florida, USA, Springer, 2007.*
3. *J. H. Reed, "Software Radio: A modern Approach to Radio Design", Pearson, 2002.*

**Reference Books**

1. *S. K. Mitra, "Digital Signal processing", Mc GrawHill, 1998*
2. *K.C.Chen and R.Prasad, "Cognitive Radio Networks", Wiley, 2009-06-15.*
3. *T. W. Rondeau, C.W.Bostian, "Artificial Intelligence in Wireless Communications", 2009.*
4. *Tusi, "Digital Techniques for Wideband receivers", Artech House, 2001.*
5. *T. DarcChiueh and P. Yun Tsai, "OFDM baseband receiver design for wireless communications", Wiley, 2007*
6. *Jerry R. Hampton, "Introduction to MIMO Communications", Cambridge University Press 2014.*
7. *Recent literature in Cognitive Radio.*

**Course outcomes**

At the end of the course student will be able to

CO1: gain knowledge on multirate systems.
CO2: develop the ability to analyze, design, and implement any application using FPGA.
CO3: be aware of how signal processing concepts can be used for efficient FPGA based system design.
CO4: understand the rapid advances in Cognitive radio technologies.
CO5: explore DDFS, CORDIC and its application.

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| **Course Code** | **:** | **EC665** |
| **Course Title** | **:** | **VLSI Process Technology** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To provide rigorous foundation in MOS and CMOS fabrication process.

**Course Content**

Electron grade silicon. Crystal growth. Wafer preparation. Vapour phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.

Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.

Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

Analytical and assembly techniques. Packaging of VLSI devices.

**Text Books**

1. *S.M.Sze, "VLSI Technology", 2nd Edition , McGraw Hill, 1988*
2. *W. Wolf, "Modern VLSI Design", 3rd Edition, Pearson,2002*

***Reference Books***

1. *James D. Plummer , "Silicon VLSI Technology: Fundamentals, Practice and Modelling", Pearson Education, 2000*
2. *Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", 2nd Edition, Oxford University Press 2001*
3. *C.Y. Chang and S.M.Sze, "ULSI Technology", McGraw Hill ,1996.*

**Course outcomes**

At the end of the course student will be able to
CO1: appreciate the various techniques involved in the VLSI fabrication process.
CO2: understand the different lithography methods and etching process.
CO3: appreciate the deposition and diffusion mechanisms.
CO4: analyze the fabrication of NMOS, CMOS memory and bipolar devices
CO5: understand the nuances of assembly and packaging of VLSI devices.

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| **Course Code** | **:** | **EC666** |
| **Course Title** | **:** | **Analysis and Design of Digital Systems using VHDL** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- To prepare the student to understand the VHDL language feature to realize the complex digital systems.
- To design and simulate sequential and concurrent techniques in VHDL
- To explain modeling of digital systems using VHDL and design methodology
- To explain predefined attributes and configurations of VHDL.
- To Understand behavioral, non-synthesizable VHDL and its role in modern design

**Course Content**

An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments. Structural specification of hardware.

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.

Data flow and behavioural description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioural description of hardware.

CPU modelling for discrete design- Parwan CPU, behavioural description, bussing structure, data flow, test bench, a more realistic Parwan. Interface design and modelling. VHDL as a modelling language.

**Text Books**

1. *Z.Navabi, "VHDL Analysis and Modelling of Digital Systems", 2nd Edition, McGraw Hill, 1998.*
2. *Perry, "VHDL", 3rd Edition, McGraw Hill.2002*

**Reference Books**

1. *A. Dewey, "Analysis and Design of Digital Systems with VHDL", CL-Engineering, 1996.*
2. *Z.Navabi, "VHDL: modular design and synthesis of cores and systems", McGraw Hill, 2007.*
3. *C. H. Roth, Jr., L.K.John, "Digital Systems Design Using VHDL" Thomson Learning EMEA Limited, 2008.*
4. *Recent literature in Analysis and Design of Digital Systems using VHDL.*

**Course outcomes**

At the end of the course student will be able to

CO1: model, simulate, verify, and synthesize with hardware description languages.
CO2: understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements.
CO3: design digital logic circuits in different types of modelling.
CO4: demonstrate timing and resource usage associated with modelling approach.
CO5: use computer-aided design tools for design of complex digital logic circuits.

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| **Course Code** | **:** | **EC667** |
| **Course Title** | **:** | **Advanced Computer Architecture** |
| **Number of Credits** | **:** | **3f** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To give an exposure on look ahead pipelining- parallelism, multiprocessor scheduling, multithreading and various memory organizations.

**Course Content**

Multiprocessors and multi-computers. Multi-vector and SIMD computers. PRAM and VLSI Models. Conditions of parallelism. Program partitioning and scheduling. Program flow mechanisms. Parallel processing applications. Speed up performance law.

Advanced processor technology. Superscalar and vector processors. Memory hierarchy technology. Virtual memory technology. Cache memory organization. Shared memory organization.

Linear pipeline processors. Non linear pipeline processors. Instruction pipeline design. Arithmetic design. Superscalar and super pipeline design. Multiprocessor system interconnects. Message passing mechanisms.

Vector Processing principle. Multivector multiprocessors. .Compound Vector processing. Principles of multithreading. Fine grain multicomputer. Scalable and multithread architectures. Dataflow and hybrid architectures.

Parallel programming models. Parallel languages and compilers. Parallel programming environments. Synchronization and multiprocessing modes. Message passing program development. Mapping programs onto multicomputer. Multiprocessor UNIX design goals. MACH/OS kernel architecture. OSF/1 architecture and applications.

**Text Books**

1. *K. Hwang, "Advanced Computer Architecture", Tata McGraw Hill, 2016.*
2. *W. Stallings, "Computer Organization and Architecture", McMillan, 2012.*

**Reference Book**

1. *M.J. Quinn, "Designing Efficient Algorithms for Parallel Computer", McGraw Hill, 1994.*
2. *Recent literature in Advanced Computer Architecture.*

**Course outcomes**

At the end of the course student will be able to
CO1: apply the basic knowledge of partitioning and scheduling in Multiprocessors.
CO2: analyze and design cache memory, virtual memory and shared memory organizations.
CO3: distinguish and analyze the design properties of Linear and Non - Linear processors.
CO4: analyze the principles of multithreading in hybrid Architectures.
CO5: write any parallel programming models for various architectures and Applications.

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| **Course Code** | **:** | **EC668** |
| **Course Title** | **:** | **Low Power VLSI Systems** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To expose the students to the low voltage device modeling, low voltage, low power VLSI CMOS circuit and system design.

**Course Content**

Evolution of CMOS technology, CMOS fabrication process, shallow trench isolation, Lightly-doped drain, Buried channel. Bi-CMOS and SOI CMOS technologies, second order effects, Modeling of MOS devices, Threshold voltage, Body effect, Short channel and Narrow channel effects, Electron temperature, MOS capacitance.

CMOS inverters, Differential static logic circuits, Pass transistor, Bi-CMOS, SOI CMOS, Low voltage and low power CMOS static logic circuit design techniques.

Basic concepts of dynamic logic circuits. Charge sharing, Noise and race problems, NORA, Zipper, Domino, Dynamic differential, BiCMOS, low voltage and low power dynamic logic techniques.

CMOS memory circuits, SRAM, DRAM, Bi-CMOS and Nonvolatile memory circuits.

Basics of clock gating and power gating. Key characteristics of the Unified Power Format (UPF) in low power design. CMOS VLSI systems, Adder circuits, Multipliers and advanced structures – PLA, PLL, DLL and processing unit.

**Text Books**

1. *J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems", Springer, 2009*
2. *J.B.KuoandJ.H.Lou, "Low-voltage CMOS VLSI Circuits", Wiley, 1999.*

**Reference Books**

1. *Michael Keating etal. "Low Power Methodology Manual For System-on-Chip Design" Springer, 2008*
2. *A.Bellaowar and M.I.Elmasry, "Low power Digital VLSI Design, Circuits and Systems", Kluwer, 1996.*
3. *IEEE Standard for Design and Verification of Low-Power, Energy- Aware Electronic Systems Sponsored by the Design Automation Standards Committee, IEEE Computer Society, 2015*

**Course outcomes**

At the end of the course student will be able to

CO1: acquire the knowledge about various CMOS fabrication process and its modelling and infer about the second order effects of MOS transistor characteristics.
CO2: analyze and implement various CMOS low voltage and low power static logic circuits.
CO3: learn the design of various CMOS low voltage and low power dynamic logic circuits.
CO4: learn the different types of memory circuits and their design.
CO5: design and implementation of various structures for low power applications.

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| **Course Code** | **:** | **EC669** |
| **Course Title** | **:** | **VLSI Digital Signal Processing Systems** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- To enable students to design VLSI systems with high speed and low power.
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

**Course Content**

An overview of DSP concepts, Representations of DSP algorithms. Systolic Architecture Design: FIR Systolic Array, Matrix-Matrix Multiplication, 2D Systolic Array Design. Digital Lattice Filter Structures: Schur Algorithm, Derivation of One-Multiplier Lattice Filter, Normalized Lattice Filter, Pipelining of Lattice Filter.

Scaling and Round off Noise - State variable description of digital filters, Scaling and Round off Noise computation, Round off Noise in Pipelined IIR Filters, Round off Noise Computation using state variable description, Slow-down, Retiming and Pipelining.

Bit level arithmetic Architectures- parallel multipliers, interleaved floor-plan and bit-plane-based digital filters, Bit serial multipliers, Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Redundant arithmetic -Redundant number representations, carry free radix-2 addition and subtraction, Hybrid radix-4 addition, Radix-2 hybrid redundant multiplication architectures, data format conversion, Redundant to Non-redundant converter.

Numerical Strength Reduction - Subexpression Elimination, Multiple Constant Multiplication, Subexpression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

**Text Book**

1. *K.K.Parhi, "VLSI Digital Signal Processing Systems", John-Wiley, 2007.*

**Reference Book**

1. *U. Meyer -Baese, "Digital Signal Processing with FPGAs", Springer, 2014.*
2. *Recent literature in VLSI Digital Signal Processing Systems.*

**Course outcomes**

At the end of the course student will be able to

CO1: explain various transforms and its corresponding architectures

CO2: describe the knowledge of effect of round off noise computation

CO3: design Bit level arithmetic Architectures and optimize the implementation of FIR filters and constant multipliers

CO4: design basic arithmetic units and realize their architecture for higher radices

CO5: create different numerical strength reduction techniques

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| **Course Code** | **:** | **EC670** |
| **Course Title** | **:** | **Asynchronous System Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- This subject introduces the fundamentals and performance of Asynchronous system
- To familiarize the dependency graphical analysis of signal transmission graphs
- To learn software languages and its syntax and operations for implementing Asynchronous Designs

**Course Content**

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

Speed-independent control circuits: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, more advanced latch control circuits.

High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

**Text Books**

1. *Chris. J. Myers, "Asynchronous Circuit Design", John Wiley and Sons, 2001.*
2. *Kees Van Berkel, "Handshake Circuits An Asynchronous architecture for VLSI programming" Cambridge University Press, 2004*

**Reference Books**

1. *Jens Sparso, Steve Furber, "Principles of Asynchronous Circuit Design", Kluwer Academic Publishers, 2001.*
2. *Richard F. Tinder, "Asynchronous Sequential Machine Design and Analysis", Morgan and Claypool Publishers, 2009*
3. *Peter A. Beerel, Recep O. Ozdag, Marcos Ferretti, "A Designer's Guide to Asynchronous VLSI", Cambridge University Press, 1st Edition, 2010*
4. *Recent literature in Asynchronous System Design.*

**Course outcomes**

At the end of the course student will be able to
CO1: understand the fundamentals of Asynchronous protocols
CO2: analyse the performance of Asynchronous System and implement handshake circuits
CO3: understand the various control circuits and Asynchronous system modules
CO4: gain the experience in using high level languages and tools for Asynchronous Design
CO5: learn commands and control flow of Balsa language for implementing Asynchronous Designs

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| **Course Code** | **:** | **EC671** |
| **Course Title** | **:** | **Advanced Digital Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- To make the students learn about graphical models and state diagram in designing optimized digital circuits.
- To provide the students a detailed knowledge of scheduling algorithm, synthesis of pipelined circuits and scheduling pipelined circuits
- To enable the students to design digital design with advanced technique like Sequential logic optimization and test the designed circuit Testability considerations.

**Course Content**

Different types of graphs. Combinational optimization- Graph optimization problems and algorithms. Boolean functions, statisfiability and cover. Abstract models, state diagrams. Data flow and sequencing graphs, compilation and behavioural optimization.

Architectural synthesis - Circuit specifications for architectural synthesis. Temporal domain, spatial domain , hierarchical models. Synchronization problems. Area and performance estimation. Strategies for architectural optimization, Data path synthesis of pipelined circuits.
Scheduling algorithms-Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits.

Resource sharing and binding. Sharing and binding for resource dominated circuits and general circuits. Concurrent binding and scheduling. Resource sharing and binding for non-scheduled sequencing graphs.

Sequential logic optimization-sequential circuit optimization using state based models and network models. Implicit finite state machine. Traversal methods. Testability considerations for synchronous circuits.

**Text Books**

1. *G.De Micheli, "Synthesis and optimization of Digital circuits", McGraw Hill, 1994 .*
2. *C. Roth, "Fundamentals of Digital Logic Design", Jaico Publishers, V ed., 2009.*
3. *Balabanian, "Digital Logic Design Principles", Wiley publication, 2007.*

**Reference Books**

1. *J. F. Wakerly, "Digital Design principles and practices", 3rd Edition, PHI publication, 1999.*
2. *S.Brown, "Fundamentals of digital logic", Tata McGraw Hill publication, 2007.*
3. *N. N. Biswas, "Logic Design Theory", Prentice Hall of India, 2001.*
4. *John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2006.*
5. *Recent literature in Advanced Digital Design.*

**Course outcomes**

At the end of the course student will be able to
CO1: understand advanced state of art techniques of digital design.
CO2: synthesis the circuits and evaluate its performance in terms of area, power and speed.
CO3: understand the use of scheduling algorithm.
CO4: gain in-depth knowledge of sequential digital circuits designed using resource sharing.
CO5: understand synchronization across clock domains, timing analysis, and Testability considerations

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| **Course Code** | **:** | **EC672** |
| **Course Title** | **:** | **Physical Design Automation** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods

**Course Content**

VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

**Text Books**

1. *S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley (India), 2006.*
2. *N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer, 2012.*

**Reference Books**

1. *S.M. Sait, H. Youssef, "VLSI Physical Design Automation", Cambridge India, 2010.*
2. *M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.*
3. *Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw Hill, 2017.*
4. *Andrew B. Kahng and Jens Lienig "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011.*
5. *Recent literature in Physical Design Automation.*

**Course outcomes**

At the end of the course student will be able to

CO1: Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.

CO2: Students are able to solve the performance issues in circuit layout.

CO3: Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing

CO4: Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing

CO5: Students are able to analyze circuits using both analytical and CAD tools

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| **Course Code** | **:** | **EC673** |
| **Course Title** | **:** | **Mixed - Signal Circuit Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To make the students to understand the design and performance measures concept of mixed signal circuit.

**Course Content**

Concepts of Mixed-Signal Design and Performance Measures. Introduction and Principle behind ADC's and DAC's - Performance Metrics of ADCs and DACs, Nyquist Rate DACs, Comparators-Characterization – Two stage comparators – open loop comparators, Nyquist rate ADCs: Flash, SAR, Pipelined, Time-interleaved ADCs. Overview of oversampling ADCs.

Design methodology for mixed signal IC design using gm/Id concept.

Design of Current mirrors. References. Comparators and Operational Amplifiers.

CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

Design of frequency and Q tunable continuous time filters.

**Text Books**

1. *David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 1997.*
2. *B. Razavi, "Principles of Data Conversion System Design", Wiley-IEEE Press, 1$^{St}$ Edition, 1994.*
3. *R. J. Baker, "CMOS Mixed Signal circuit Design", Wiley-IEEE Press, 2$^{nd}$ Edition, 2008.*
4. *M.Gustavsson, J. J. Wikner, and N. N. Tan, "CMOS Data Conversion for Communications", Springer; 2000*

**Course outcomes**

At the end of the course student will be able to
CO1: appreciate the fundamentals of data converters and also optimized their performances.
CO2: understand the design methodology for mixed signal IC design using gm/Id concept.
CO3: analyze the design of current mirrors and operational amplifiers
CO4: design the CMOS digital circuits and implement its layout.
CO5: design the frequency and Q-tunable time domain filters.

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| **Course Code** | **:** | **EC674** |
| **Course Title** | **:** | **RF Circuits** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objectives**

- To impart knowledge on basics of CMOS IC design at RF frequencies.
- To be familiar with the circuits used in RF front end in transceiver design.

**Course Content**

Overview of RF Systems: Wireless Transmitter and Receiver Architecture – Heterodyne and Super-Heterodyne Systems - Basic concepts in RF design - units in RF Design, time variance - Effects of Nonlinearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion - Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, representation of noise in circuits.

High frequency amplifier design – Types of amplifiers: Narrowband and Wideband Amplifiers - zeros as bandwidth enhancers, shunt-series amplifier, $f_T$ doublers, neutralization and unilateralization

Need for LNA: Friis' equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA topology - linearity and large signal performance

Need for Mixers – Noise and Linearity trade-off in RF Mixer design - traditional mixer circuits: multiplier-based mixers, subsampling mixers, diode-ring mixers - Noise Folding - Single-sideband and Double-sideband Noise Figure – Feedthrough: Single balanced and Double Balanced – IP3 and IP2 improvement - Oscillators and synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.

RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations. RFIC simulation and layout- General Layout Issues, Passive and Active Component Layout.

**Text Books**

1. *Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd Edition, Cambridge University Press, 2004.*
2. *B. Razavi, "RF Microelectronics", 2nd Edition, Prentice Hall, 1998.*

**Reference Books**

1. *A. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 1999.*
2. *R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson, 2000.*
3. *Mattuck,A., "Introduction to Analysis", Prentice-Hall,1998.*

**Course outcomes**

At the end of the course student will be able to

CO1: understand the basics of RF system design and analyse the high frequency amplifier design
CO2: appreciate the need for LNA and learn different LNA topologies and design techniques
CO3: understand the requirement of RF Mixer, its function and performance parameters
CO4: analyse the various types of synthesizers, oscillators and their characteristics.
CO5: learn about the need for power amplifiers and the effects of nonlinearities

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| **Course Code** | **:** | **EC675** |
| **Course Title** | **:** | **Functional Verification using Hardware Verification Languages** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To expose the students to all aspects of functional verification of digital systems

**Course Content**

System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks and Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads and Inter Process Communication, Advanced OOPs and Test bench guidelines, Advanced Interfaces.

A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modelling with SV, Connecting Test bench and Design, Behavioral and Transaction Level Modelling with SV

System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single and Multiple Clock definitions, Implication operators (Overlapping and Non-overlapping), Repetition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property.

SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, Assertions: Practice and Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.

Functional Verification coverage using design, verification languages and implementation standards: Verilog IEEE 1364, VHDL IEEE 1076, System Verilog IEEE 1800, Property Specific Language (PSL) IEEE 1850, System C™ IEEE 1666, Encryption IEEE 1735, *e* Verification Language IEEE 1647, Open Verification Methodology (OVM) and Universal Verification Methodology (UVM).

**Text Books**

1. *Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for design: a guide to using System Verilog for hardware design and modelling", Springer, 2004.*
2. *Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", Springer, 2008.*
3. *Srikanth Vijayaraghavan and Meyyappan Ramanathan, "A Practical guide for System Verilog Assertions", Springer, 2005.*

**Reference Books**

1. *Janick Bergeron, "Writing test benches using System Verilog", Birkhäuser, 2006.*
2. *Ben Cohen, cohen, Venkataramanan, Kumari, Srinivasan Venkataramanan, Ajeetha Kumari, "SystemVerilog Assertions Handbook: for Formal and Dynamic Verification", vhdl cohen publishing, 2005.*
3. *Recent literature in Functional Verification using Hardware Verification Languages.*

**Course outcomes**

At the end of the course student will be able to

CO1: To learn about the testing environment of digital systems
CO2: To create test benches for digital systems
CO3: To learn about verification methodologies
CO4: To understand the need for system verification
CO5: To acquire digital verification skills

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| **Course Code** | **:** | **EC676** |
| **Course Title** | **:** | **Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To expose the students to all aspects of testing analog/mixed-signal circuits.

**Course Content**

Overview of Mixed-signal Testing. DC and Parametric Measurements. DAC Testing: Basics of converter testing, Basic DC tests, Transfer curve tests, Dynamic DAC tests, DAC Architectures.

ADC Testing: ADC testing versus DAC testing, DC tests and Transfer curve tests, Dynamic ADC tests, ADC Architectures. Sampling Theory. DSP based testing: Advantages of DSP based testing, DSP, Discrete-time transforms, The Inverse FFT.

Analog Channel Testing. Fundamentals of RF Testing. Design for Test: Overview, Advantages of DFT, Digital Scan, Digital BIST, Digital DFT for Mixed-signal circuits, Mixed-signal boundary scan and BIST, Ad-hoc Mixed signal DFT, RF DFT.

High speed design techniques: High Speed Op-amps, High Speed op-amp applications, RF/IF Subsystems.

High Speed sampling and High Speed ADCs, High Speed DACs and DDS systems.

**Text Books**

1. *An Introduction to Mixed-signal IC test and Measurement - Mark Burns, Gordon W. Roberts*
2. *High Speed Design Techniques - Walt Kester, Analog Devices*

**Reference Books**

1. *Linda S. Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing", IEEE Transactions on circuits and systems-II: Analog and Digital signal processing, Vol. 45, No. 10, October 1998.*
2. *The Fundamentals of Mixed Signal Testing - Brian Lowe*
3. *Test and Design for Testability in Mixed Signal ICs - Jose L Huertas*
4. *High Speed* Analog Design and Application Seminar - Texas Instruments.
5. *Recent literature in Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design.*

**Course outcomes**

At the end of the course student will be able to
CO1: To understand the testing methodology
CO2: To build test systems
CO3: To understand the requirements for BIST
CO4: To learn about error correction mechanisms
CO5: To understand the benefits of BIST

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| **Course Code** | **:** | **EC677** |
| **Course Title** | **:** | **High Speed System Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To expose the students to all aspects of electronic packaging including electrical, thermal, mechanical and reliability issues.

**Course Content**

Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates

Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and nonideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise.

Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Design Process Electrical Design: Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines , Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining.

IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging , reliability, wafer level burn – in and test.Single chip packaging : functions, types, materials processes, properties, characteristics, trends.Multi chip packaging : types, design, comparison, trends. Passives: discrete, integrated, embedded –encapsulation and sealing: fundamentals, requirements, materials, processes

Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation – Cooling requirements.

Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue – failures – thermo mechanically induced – electrically induced – chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

**Text Book**


1. *Tummala, Rao R., "Fundamentals of Microsystems Packaging", McGraw Hill, 2001*
2. *Howard Johnson , Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993*


**Reference Books**


1. *Blackwell (Ed), "The electronic packaging handbook", CRC Press, 2000.*
2. *Tummala, Rao R, "Microelectronics packaging handbook", McGraw Hill, 2008.*
3. *Bosshart, "Printed Circuit Boards Design and Technology", Tata McGraw Hill, 1988.*

4. *R.G. Kaduskar and V.B.Baru, "Electronic Product design", Wiley India, 2011*
5. *R.S.Khandpur, "Printed Circuit Board", Tata McGraw Hill, 2005*
6. *Recent literature in Electronic Packaging***.**

**Course outcomes**

At the end of the course student will be able to

CO1: design of PCBs which minimize the EMI and operate at higher frequency.

CO2: design of packages which can withstand higher temperature, vibrations and shock.

CO3: explain the basic techniques for statistical process control and failure mode and effect analysis.

CO4: prescribe and perform parametric test and analysis and the troubleshooting of electronic circuits with the application of basic and virtual electronic instruments

CO5: explain contemporary pragmatic manufacturing processes, interconnects and assembly methods for electronic equipment fabrication.

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| **Course Code** | **:** | **EC678** |
| **Course Title** | **:** | **Modelling of Solid-State Circuits** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Objectives**

- To study and model MOS Transistors and MOS Capacitors
- To understand the various CMOS design parameters and their impact on performance of the device.
- To study the device level characteristics of BJT transistors

**Course Content**

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non-equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunnelling, Tunnelling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields.

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Non-scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non-uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS
n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non-ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages,

Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between $B_{VCEO}$ and $B_{VCBO}$.

**Reference Books:**

1. *Behzad Razavi, "Fundamentals of Microelectronics", Wiley Student Edition, 2nd Edition, 2008.*
*2. J P Collinge, C A Collinge, "Physics of Semiconductor devices" Springer 2002 Edition.*
*3. Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition, 2009.*

**Course outcomes**

At the end of the course student will be able to
CO1: To design and model MOSFET and BJT devices to desired specifications.
CO2: To understand the physics behind the device operation
CO3: To analyse the impact of the device physics in circuit design
CO4: To model novel semiconductor devices
CO5: To analyse the working of deep submicron semiconductor devices.

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| **Course Code** | **:** | **EC679** |
| **Course Title** | **:** | **Nano-Scale Devices: Modelling and Circuits** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Objectives**

- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano-scaled MOS transistor circuits

**Course Content**

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

Silicon nanowire MOSFETs – Evaluation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors

Radiation effects in SOI MOSFETs, total ionizing dose effects – single-gate SOI – multi-gate devices, single event effect, scaling effects

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

**Reference Books:**

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modelling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000

**Course Outcomes**

At the end of the course student will be able to

CO1: study the MOS devices used below 10nm and beyond with an eye on the future
CO2: understand and study the physics behind the operation of multi-gate systems.
CO3: design circuits using nano-scaled MOS transistors with the physical insight of their functional characteristics
CO4: To appreciate the growth of scaling in MOSFETs
CO5: To understand the physical effects in deep sub-micron MOS devices

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| **Course Code** | **:** | **EC680** |
| **Course Title** | **:** | **Embedded System Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Objective**

- Ability to understand the technologies and techniques underlying in developing an embedded system.

**Course Content**

Introduction to Embedded system, embedded system examples, Parts of Embedded System Typical Processor architecture, Power supply, clock, Cache memory, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC etc. Bus architecture -$I^2C$, SPI, AMBA, CAN. Memory Technologies – EPROM, Flash, OTP, SRAM, DRAM, SDRAM etc.

Introduction to Cypress Programmable System on Chip (PSoC). Structure of PSoC, PSoC Designer, PSoC Modules, Interconnects, Memory Management, Global Resources, Design Examples
Embedded System product Development Life cycle (EDLC), Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure Design and Development. Concept of firmware, operating system and application programs. Power supply Design. External Interfaces.
Basic Features of an Operating System, Kernel Features [polled loop system, interrupt driven system, multi rate system], Processes and Threads, Context Switching, Scheduling[RMA, EDF, fault tolerant scheduling], Inter-process Communication, real Time memory management [process stack management, dynamic allocation], I/O [synchronous and asynchronous I/O, Interrupts Handling, Device drivers], RTOS [ VxWorks, RT-LINUX].

Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT) etc.

**Text Books**


*1. Shibu, "K.V. Introduction to Embedded Systems", Tata McGraw Hill, 2009*
*2. Marilyn Wolf, "Computers as components: Principles of Embedded Computing System Design" Elsevier, 2012.*
*3. Raj Kamal, "Embedded systems Architecture, Programming and Design", 2nd Edition, 2008*
*4. Lyla B Das, "Embedded Systems: An Integrated Approach", Pearson, 2013*
*5. Robert Ashby, "Designer's Guide to the Cypress PSoC Newnes", An imprint of Elsevier, 2006.*
*6. Oliver H. Bailey, "The Beginner's Guide to PSoC Express" Timelines Industries Inc., 1st Edition, 2007.*


**Course outcomes**

At the end of the course student will be able to
CO1: define an embedded system and compare with general purpose system.
CO2: appreciate the methods adapted for the development of a typical embedded system.
CO3: get introduced to RTOS and related mechanisms.
CO4: To build embedded systems for real-time applications
CO5: To debug digital embedded systems and solve complex problems.

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| **Course Code** | **:** | **EC681** |
| **Course Title** | **:** | **Internet of Things** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Objective**

- To give an exposure on the infrastructure, sensor technologies and networking technologies of IoT.
- To analyse, design and develop IOT solutions.
- To apply the concept of Internet of Things in the real world scenarios.

**Course Content**

Definition and Characteristics of IoT - Challenges and Issues - Physical Design of IoT, Logical Design of IoT - IoT Functional Blocks, Security.

Control Units – Communication modules – Bluetooth – Zigbee – Wifi – GPS- IOT Protocols (IPv6, 6LoWPAN, RPL, CoAP etc.), MQTT, Wired Communication, Power Sources.

Four pillars of IOT paradigm, - RFID, Wireless Sensor Networks, SCADA (Supervisory Control and Data Acquisition), M2M - IOT Enabling Technologies - BigData Analytics, Cloud Computing, Embedded Systems.

Working principles of sensors – IOT deployment for Raspberry Pi /Arduino/Equivalent platform – Reading from Sensors, Communication: Connecting microcontroller with mobile devices – communication through Bluetooth, wifi and USB - Contiki OSCooja Simulator.

Clustering, Clustering for Scalability, Clustering Protocols for IOT.

The Future Web of Things – Set up cloud environment –Cloud access from sensors– Data Analytics for IOT- Case studies- Open Source ‘e-Health sensor platform’ – ‘Be Close Elderly monitoring’ – Other recent projects.

**Text Books**

1. *Dieter Uckelmann et.al, “Architecting the Internet of Things”, Springer, 2011*
2. *Arshdeep Bahga and Vijay Madisetti, “Internet of Things – A Hand-on Approach”, Universities press, 2015.*

**Reference Book**

1. *Charalampos Doukas , “Building Internet of Things with the Arduino,"Create space, April 2002*
2. *Dr. Ovidiu Vermesan and Dr. Peter Friess, “Internet of Things: From research and innovation to market deployment”, River Publishers 2014.*
3. *Contiki: The open source for IOT, www.contiki-os.org*

**Course outcomes**

At the end of the course student will be able to
CO1: identify the components of Internet of Things
CO2: development of IoT based application.
CO3: Build IoT based platforms for various use cases
CO4: Study the data gathered by IoT devices
CO5: Predict and dynamically optimize systems based on IoT data

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| **Course Code** | **:** | **EC682** |
| **Course Title** | **:** | **Semiconductor Memories** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Contents:**

Memory hierarchy in digital systems; Static RAM: Types, Overall architecture, SRAM Cell - Design, Layout, Noise Issues and Margins and Assembly of Core, Peripheral Circuitry - Decoding, Array conditioning for read/write, Sensing, Writing, Synchronization;

Dynamic RAM: Types, Cell design, Assembly of core, Core architectures, Peripheral circuitry - Sensing, Elevated voltage supplies; Modern high speed DRAM - EDO, SDR, DDR;

Non Volatile Memories: ROM - Array Design, EPROM - Cell and Array Design, EEPROM - Tunnelling Phenomena, EEPROM Cell both Hot Carrier based operation and Tunnelling based Operation;

Flash Memories: Cell operation and design, Types of modern high density flash memories - NOR Flash, NAND Flash.

**Reference Books:**


1. *Betty Prince, "Semiconductor Memories: A Handbook of Design, Manufacture and Application", 2nd Edition, John Wiley,1996.*
2. *Betty Prince, "High Performance Memories: New Architecture DRAMs and SRAMs – Evolution and Function", Johm Wiley, 1999*
3. *Kiyoo Itoh, Masashi Horiguchi and Hitoshi Tanak, "Ultra-Low Voltage Nano-Scale Memories"' Springer International Edition, 2007*


**Course outcomes**

At the end of the course student will be able to

CO1: identify the parts of Memories

CO2: development of Semiconductor Memory architectures.

CO3: To learn the fundamental problems in memory design

CO4: develop novel circuit techniques for improving memory design

CO5: To understand and appreciate the growing semiconductor market for memory

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| **Course Code** | **:** | **EC683** |
| **Course Title** | **:** | **FPGA Based System Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To enable the students to understand the design and performance measures of FPGA based system design

**Course Content**

Decimation and Interpolation. Spectrum of decimated and interpolated signals, Polyphase decomposition of FIR filters and its applications to multirate DSP. Cascade equivalence (Noble identity). Sampling rate converters. Band pass sampling theorem. Sub-band encoder.

Uniform filter bank: Direct and DFT approach. Introduction to ADSL Modem. Discrete Multitone modulation and its realization using DFT. QMF. Condition for perfect reconstruction for two channel filter bank. Computation of discrete wavelet transform using filter banks. Design considerations for filters used in sub-band encoders and DWT computers.

Linear Adaptive filtering. Method of steepest descent. Least-mean-square algorithm. Frequency domain adaptive filters. Method of least squares. Recursive least-square algorithm. Square-Root adaptive filters. Order-Recursive adaptive filters. Nonlinear adaptive filtering.

Analog signal synthesis and its limitations, Introduction to direct digital synthesis. ROM look up table approach. Phase truncation distortion. Analysis of the output sequence. Analysis of spurious signals. Periodic components due to jitter. Hybrid approach for waveform generation. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC. CORDIC architectures. Universal modulator using CORDIC.

Block diagram of a software radio, Universal demodulator using CORDIC, Incoherent demodulation: Analog I and Q down converters. Digital approach for I and Q generation. Narrowband and wideband I and Q channels through special sampling scheme. Hardware design considerations on filter design for digital I, Q channels, CIC filters. Residue number system and high speed filters using RNS. Down conversion using Discrete Hilbert transform. Coherent Demodulation: Linear PLL, Digital PLL, Carrier synchronization: squaring loops, Costas loop, Clock synchronization.

**Text Book**

1. *S. K. Mitra, "Digital Signal processing", McGraw Hill, 1998*
2. *J. H. Reed, "Software Radio", Pearson Education, 2002.*
3. *U. Meyer – Baese, "Digital Signal Processing with FPGAs", Springer Verlag, 2001*

**Reference Books**

1. Simon Haykin, "Adaptive filter theory and applications", 4th Edition, Pearson, 2002
2. W.Tuttlebee, "Software defined radio: Baseband technology for 3G", Wiley, 2004
3. J. Tsui, "Digital Techniques for Wideband Receivers", Artech House, 1995.
4. *C. Chien, "Digital Radio Systems on a Chip", Kluwer, 2001.*

**Course outcomes**

At the end of the course student will be able to

CO1: acquire the basics of Multi rate Digital Signal Processing.
CO2: understand the concepts of Filter Banks and its applications.
CO3: understand the concepts and algorithms of Adaptive Filter theory.
CO4: understand the basics of Digital waveform synthesis and appreciate its applicability to various communication systems.
CO5: understand the concepts of Digital Down converters and Demodulators.

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| **Course Code** | **:** | **EC684** |
| **Course Title** | **:** | **Bio-Medical CMOS ICs** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To develop skills to design biomedical IC circuits

**Course Content**

Introduction to Bio-Medical CMOS Ics: Introduction to Bioelectricity, Electrical Properties of the Human body, Equivalent Circuit Model of Tissues and Organs, Biomedical Devices, Current Research Trends in Biomedical Electrical Instruments.

Electrode Design, Modern Disposable Electrodes, Solid Conductive Adhesive Electrodes, Implant Electrodes, Microelectrodes, Electrode Standards.

Readout circuits: Biopotential Acquisition, Power Efficient Instrumentation Amplifier Topologies for Biopotential Signal Extraction, Current Mode Instrumentation Amplifiers,
Examples of ICs for Biopotential Acquisition.

Basic operation principles and architectures as well as the most recent research results of low power CMOS ICs. Low power ADCs for Bio-Medical Applications, Low Power Bio-Medical DSP.

Bio-Medical Wireless Communication, Introduction to Short distance Wireless Communications.

**Text Books**

1. *Hoi-Jun Yoo: Chris van Hoof , "Integrated Circuits and Systems- Bio Medical CMOS ICs", Springer, 2010*
2. *D C Reddy "Biomedical Signal Processing: Principles and Techniques", Tata McGraw-Hill Publishing Co. Ltd, 2005*

**Reference Books**

1. *R M Rangayyan, "Biomedical Signal Analysis: A case Based Approach", IEEE Press, John Wiley and Sons. Inc., 2002*
2. *Jacob Fraden, "Handbook of Modern Sensors: Physics, Designs, and Applications", Springer, 2010*
3. *J. G. Webster, "The Measurement, Instrumentation and Sensors Handbook vol. 1", CRC Press, 1st Edition, 1998*

**Course outcomes**

At the end of the course student will be able to

CO1: familiarise the concepts of used to design biomedical ICs
CO2: acquire knowledge to design various electrodes
CO3: learn the design of various biomedical amplifiers
CO4: analyse and implement various low power ADCs for biomedical applications
CO5: acquire knowledge about types of short range wireless communication

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| **Course Code** | **:** | **EC685** |
| **Course Title** | **:** | **On-chip Antenna Design** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To make the students understand the basic concepts and design procedures of on-chip antennas.
- Introduce the students to various packaging technologies for on-chip antennas

**Course Content**

Introduction to millimetre wave technologies: Antenna, RF Electronics, Packaging, Millimetre wave packaging, Review of Microwave Packaging Technologies, Low-cost mm Wave Packaging, Emerging Packaging Technologies, Package Co-design at mm Waves.

Millimetre-wave Interconnects: Interconnects at Millimetre-wave Frequencies, Interconnect Technology Options for Millimetre-wave Applications, Performance-oriented Interconnect Technology Optimization, Chip-to-package Interconnects at Millimetre-wave Frequencies.

Printed Millimetre Antennas: Introduction and Considerations for Millimetre-wave Printed Antennas, Multilayer Interconnection Technology, Multilayer Antenna Array with Shaped Beam, Connector and Diffraction Problems for Printed Antennas.

Planar Waveguide-type Slot Arrays: Equivalent Length of a Round-ended Straight Slot, Alternating-phase Fed Single-layer Slotted Waveguide Array and its Side lobe Suppression, Centre Feed Single Layer Slotted Waveguide Array, Single-layer Hollow-waveguide Eight-way Butler Matrix, Radial Line Slot Antennas, Post-wall Waveguide-fed Parallel Plate Slot Arrays, Coaxial-line to Post-wall Waveguide Transformers.

Antenna Design for Packaging Applications: Air-suspended Superstrate Antenna, Packaged Antennas, A Patch Array, Circularly Polarized Antenna, Assembly Process, Advanced Packaging Application. Monolithic Integrated Antennas: Monolithic Antenna Integration Challenges, Manufacturing Techniques for Enhanced Antenna Performance, Circuit Integration, Packaging of Integrated Circuits with On-chip Antennas, Monolithic Antenna Measurement Techniques.
Phased Array: Antenna Element Design for Phased Arrays, Beam-forming Network, Design and Manufacture Issues Integrated Phased Arrays: Integrated Phased Arrays, Fully Integrated mm Wave Phased-array Transceiver, Direct Antenna Modulation, Large-scale Integrated Phased Arrays. CMOS RF Circuits- Integrated Transmitter and Receiver, Wireless Inter chip Interconnects.

**Text Books**

1. *Duixian Liu, Brian Gaucher, "Advanced millimetre wave technologies: Antennas, Packaging and Circuits", Wiley, 2012.*
2. *Mikhail R. Baklanov, Paul S. Ho, EhrenfriedZschech, "Advanced interconnects for ULSI Technology", Wiley, 2012.*

**Reference Books**

1) *Samee Ullah Khan, Joanna Kołodziej, Juan Li, Albert Y. Zomaya, "Evolutionary based solutions for green computing", Springer 2013.*

**Course outcomes**

At the end of the course student will be able to

CO1: Familiarise the effects of substrates on millimetre wave antennas
CO2: Design of interconnects at millimetre wave frequencies
CO3: Design millimetre wave printed antennas antennas
CO4: Enable design of antennas with packages
CO5: Acquire knowledge about antenna arrays and phased arrays

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| **Course Code** | **:** | **EC612** |
| **Course Title** | **:** | **DSP Architecture** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors.

**Course Content**

Fixed-point DSP architectures. TMS320C54X, ADSP21XX, DSP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses. TMS320C55X architecture and its comparison.

Floating-point DSP architectures. TMS320C67X, DSP96XX architectures. Cache architecture. Floating-point Data formats. On-chip peripherals. Memory Map and Buses.

On-chip peripherals and interfacing. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF. Serial interface- Audio codec. Sensors. A/D and D/A interfaces. Parallel interface- RAM and FPGA. RF transceiver interface.

DSP tools and applications. Implementation of Filters, DFT, QPSK Modem, Speech processing. Video processing, Video Encoding / Decoding. Biometrics. Machine Vision. High performance computing (HPC).

Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP. CORTEX, SHARC, SIMD, MIMD Architectures.

**Text Books**

1. *B.VenkataramaniandM.Bhaskar, "Digital Signal Processor, Architecture, Programming and Applications", 2nd Edition, McGraw- Hill,2010*
2. *S.SrinivasanandAvtar Singh, "Digital Signal Processing, Implementations using DSP Microprocessors with Examples from TMS320C54X", Brooks/Cole, 2004*

**Reference Books**

1. *S.M.KuoandWoon-Seng S.Gan, "Digital Signal Processors: Architectures, Implementations, and Applications", Prentice Hall, 2004.*
2. *N. Kehtarnavazand M. Kerama, "DSP System Design using the TMS320C6000", Prentice Hall, 2001.*
3. *S.M. KuoandB. H.Lee, "Real-Time Digital Signal Processing, Implementations, Applications and Experiments with the TMS320C55X", John Wiley, 2001.*
4. *Recent literature in DSP Architecture.*

**Course outcomes**

At the end of the course student will be able to

CO1: learn the architecture details fixed and floating point DSPs

CO2: infer about the control instructions, interrupts, and pipeline operations, memory and buses.

CO3: illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.

CO4: learn to implement the signal processing algorithms and applications in DSPs.

CO5: learn the architecture of advanced DSPs.

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| **Course Code** | **:** | **EC613** |
| **Course Title** | **:** | **High Speed Communication Networks** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To impart the students a thorough exposure to the various high speed networking technologies and to analyze the methods adopted for performance modeling , traffic management and routing

**Course Content**

The need for a protocol architecture, The TCP/IP protocol architecture, Internetworking,
Packet switching networks, Frame relay networks, Asynchronous Transfer mode (ATM) protocol architecture, High speed LANs. Multistage networks

Overview of probability and stochastic process, Queuing analysis, single server and multi-server queues, queues with priorities, networks of queues, Self similar Data traffic

Congestion control in data networks and internets, Link level flow and error control, TCP traffic control, Traffic and congestion control in ATM networks

Overview of Graph theory and least cost paths, Interior routing protocols, Exterior routing protocols and multicast.

Quality of service in IP networks, Integrated and differentiated services, Protocols for QOS support-Resource reservation protocol, Multiprotocol label switching, Real time transport protocol.

**Text Books**

1. *W. Stallings," High Speed networks and Internets", second edition, Pearson Education, 2002.*
2. *A. Pattavina,"Switching Theory", Wiley, 1998.*
3. *J. F. Kurose and K. W. Ross, "Computer networking", 3rd Edition, Pearson education,2005*

**Reference Books**

1. *Mischa Schwartz, "Telecommunication networks, protocols, modeling and analysis", Pearson education,2004*
2. *Giroux, N. and Ganti, S, "Quality of service in ATM networks", Prentice Hall ,1999*
3. *Recent literature in High Speed Communication Networks.*

**Course outcomes**

At the end of the course student will be able to

CO1: compare and analyze the fundamental principles of various high speed communication networks and their protocol architectures
CO 2: analyze the methods adopted for performance modeling of traffic flow and estimation
CO 3: examine the congestion control issues and traffic management in TCP/IP and ATM networks
CO 4: compare, analyze and implement the various routing protocols in simulation software tools
CO 5: examine the various services.

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| **Course Code** | **:** | **EC615** |
| **Course Title** | **:** | **Digital Image Processing** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To explore various techniques involved in Digital Image Processing.

**Course Content**

Elements of Visual perception. Image sensing and Acquisition. Imaging in different bands. Digital Image Representation. Relationship between pixels. Image transformations: 2D-DFT, DCT, DST, Hadamard, Walsh, Hotelling transformation, 2D-Wavelet transformation, Wavelet packets.

Image Enhancements in spatial domain and Frequency domain. Image Restoration techniques. Color Image processing.

Error free compression: Variable length coding, LZW, Bit-plane coding, Lossless predictive coding Lossy compression: Lossy predictive coding, transform coding, wavelet coding. Image compression standards (CCITT, JPEG, JPEG 2000) and Video compression standards.

Summary of morphological operations in Binary and Gray Images. Image segmentation: Point, Line and Edge segmentation. Edge linking and Boundary detection. Segmentation using thresholding, Region based segmentation. Segmentation by morphological watersheds. Use of motion in segmentation.

Feature Extraction from the Image: Boundary descriptors, Regional descriptors, Relational descriptors. Dimensionality reduction techniques, Discriminative approach and the Probabilistic approach for image pattern recognition.

**Text Books**

1. *R. C.Gonzalez, R.E.Woods," Digital Image processing", Pearson edition, Inc3/e, 2008.*
2. *A.K.Jain," Fundamentals of Digital Image Processing", PHI,1995*

**Reference Books**

1. *J.C. Russ, "The Image Processing Handbook", 5th Edition, CRC, 2006*
2. *R.C.Gonzalez and R.E. Woods; "Digital Image Processing with MATLAB", Prentice Hall, 2003*
3. *E.S.Gopi, "Digital Image processing using Matlab", Scitech publications, 2005*
4. *Recent literature in Digital Image Processing***.**

**Course outcomes**

At the end of the course student will be able to

CO1: understand the need for image transforms different types of image transforms and their properties.
CO2: develop any image processing application.
CO3: understand the rapid advances in Machine vision.
CO4: learn different techniques employed for the enhancement of images.
CO5: learn different causes for image degradation and overview of image restoration techniques.

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| **Course Code** | **:** | **EC616** |
| **Course Title** | **:** | **RF MEMS** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To impart knowledge on basics of MEMS and their applications in RF circuit design.

**Course Content**

Micromachining Processes - methods, RF MEMS relays and switches. Switch parameters. Actuation mechanisms. Bistable relays and micro actuators. Dynamics of switching operation.

MEMS inductors and capacitors. Micro-machined inductor. Effect of inductor layout. Modelling and design issues of planar inductor. Gap-tuning and area-tuning capacitors. Dielectric tunable capacitors.

MEMS phase shifters. Types. Limitations. Switched delay lines. Fundamentals of RF MEMS Filters.

Micro-machined transmission lines. Coplanar lines. Micro-machined directional coupler and mixer.

Micro-machined antennas. Microstrip antennas – design parameters. Micromachining to improve performance. Reconfigurable antennas.

**Text Book**

1. *Vijay. K. Varadan, K.J. Vinoy, and K.A. Jose, "RF MEMS and their Applications", Wiley-India, 2011.*

**Reference Books**

1. *H. J. D. Santos, "RF MEMS Circuit Design for Wireless Communications", Artech House, 2002.*
2. *G. M. Rebeiz, "RF MEMS Theory, Design, and Technology", Wiley, 2003.*
3. *Recent literature in RF MEMS.*

**Course outcomes**

At the end of the course student will be able to
CO1: learn the Micromachining Processes
CO2: learn the design and applications of RF MEMS inductors and capacitors.
CO3: learn about RF MEMS Filters and RF MEMS Phase Shifters.
CO4: learn about the suitability of micro-machined transmission lines for RF MEMS
CO5: learn about the Micro-machined Antennas and Reconfigurable Antennas.

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| **Course Code** | **:** | **EC626** |
| **Course Title** | **:** | **Bio MEMS** |
| **Number of Credits** | **:** | **3** |
| **Course Type** | **:** | **Elective** |

**Course Learning Objective**

- To train the students in the design aspects of Bio MEMS devices and Systems. To make the students aware of applications in various medical specialists especially the Comparison of conventions methods and Bio MEMS usage.

**Course Content**

Introduction-The driving force behind Biomedical Applications – Biocompatibility - Reliability Considerations-Regularity Considerations – Organizations - Education of Bio MEMS-Silicon Micro fabrication-Soft Fabrication techniques

Micro fluidic Principles- Introduction-Transport Processes- Electro kinetic Phenomena-Micro valves – Micro mixers- Micro pumps.

SENSOR PRINCIPLES and MICRO SENSORS: Introduction-Fabrication-Basic Sensors-Optical fibers-Piezo electricity and SAW devices-Electrochemical detection-Applications in Medicine

MICRO ACTUATORS and DRUG DELIVERY: Introduction-Activation Methods-Micro actuators for Micro fluidics-equivalent circuit representation-Drug Delivery

MICRO TOTAL ANALYSIS: Lab on Chip-Capillary Electrophoresis Arrays-cell, molecule and Particle Handling-Surface Modification-Microsphere-Cell based Bioassay Systems
Detection and Measurement Methods-Emerging Bio MEMS Technology-Packaging, Power, Data and RF Safety-Biocompatibility, Standards

**Text Book**

1. *Steven S. Saliterman, "Fundamentals of Bio MEMS and Medical Micro devices", Wiley Inter science, 2006.*

**Reference Books**

1. *Albert Folch , "Introduction to Bio MEMS", CRC Press, 2012*
2. *Gerald A. Urban, "Bio MEMS", Springer, 2006*
3. *Wanjun wang, steven A. Soper, "Bio MEMS", 1st Edition, CRC Press, 2006.*
4. *M. J. Madou, "Fundamental of Micro fabrication", 2nd Edition, CRC Press, 2002.*
5. *G.T. A. Kovacs, "Micro machined Transducers Sourcebook", 1st Edition, McGraw Hill, 1998.*
6. *Recent literature in Bio MEMS.*

**Course outcomes**

At the end of the course student will be able to
CO1: learn and realize the MEMS applications in Bio Medical Engineering
CO2: understand the Micro fluidic Principles and study its applications.
CO3: learn the applications of Sensors in Health Engineering.
CO4: learn the principles of Micro Actuators and Drug Delivery system
CO5: learn the principles and applications of Micro Total Analysis