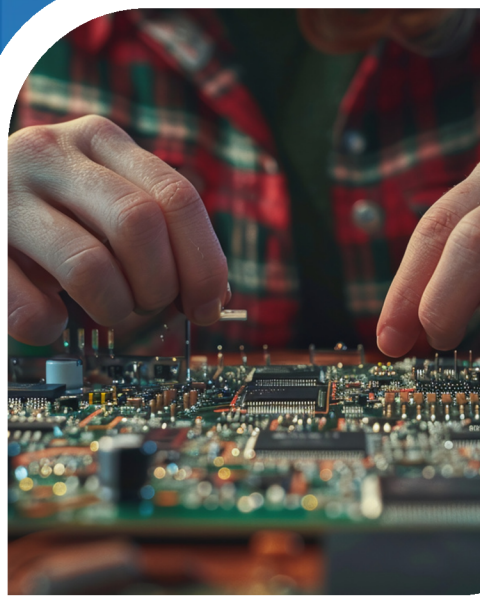
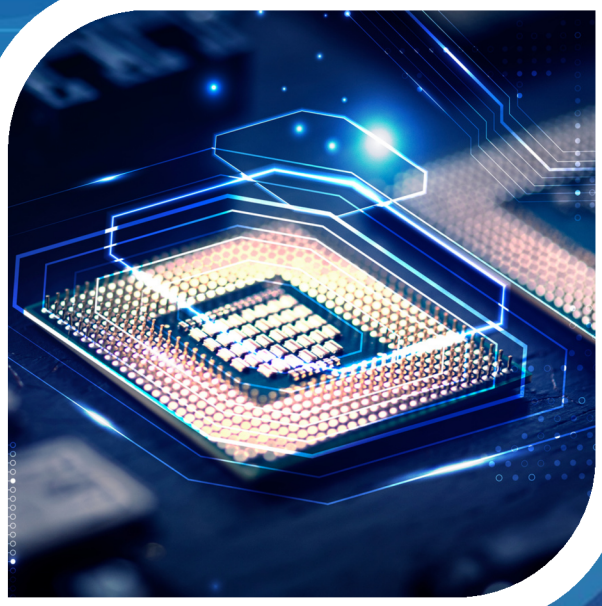
DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

MASTER OF TECHNOLOGY
V.L.S.I. SYSTEM

CURRICULUM

[EFFECTIVE FROM 2024 – 25 ONWARDS]





NATIONAL INSTITUTE OF TECHNOLOGY
TIRUCHIRAPPALLI – 620 015

Institute Vision and Mission

Vision

- To be a university globally trusted for technical excellence where learning and research integrate to sustain society and industry.

Mission

- To offer undergraduate, postgraduate, doctoral and modular programmes in multi-disciplinary / inter-disciplinary and emerging areas.
- To create a converging learning environment to serve a dynamically evolving society.
- To promote innovation for sustainable solutions by forging global collaborations with academia and industry in cutting-edge research.
- To be an intellectual ecosystem where human capabilities can develop holistically.

Department Vision and Mission

Vision

- To excel in education and research in Electronics and Communication Engineering

Mission

- To educate with the state of art technologies to meet the growing challenges of the industry.
- To carry out research through constant interaction with research organizations and industry.
- To equip the students with strong foundations to enable them for continuing Education.

Program Educational Objectives (PEOs)

- **PEO1:** Graduates will be successful in facing the challenges in their professional career in industry, government and academia by integrating the existing and advanced knowledge in VLSI Systems to solve complex problems in Electronics and Communication engineering.

- **PEO2:** Graduates will be efficient in adapting new technologies, achieve excellence in their professional career, lead research as well as development projects/activities and establish themselves as successful professional.

- **PEO3:** Graduates will practice and inspire high ethical and technical standards, possess technical competency in VLSI Systems and take up higher studies.

Program Outcomes (POs)

- **PO1:** An ability to independently carry out research /investigation and development work to solve practical problems in VLSI System.

- **PO2:** An ability to write and present a substantial technical report/document in VLSI System.

- **PO3:** Students should be able to demonstrate mastery over VLSI System. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

CURRICULUM

The total minimum credits for completing the M.Tech. Programme in VLSI System is 80.

SEMESTER I

Sl. No.	Course Code	Course of	Credits
1.	EC651	Analog VLSI	4
2.	EC653	Basics of VLSI	4
3.	EC661	Digital System Design	4
4.		Elective I	3
5.		Elective II	3
6.		Elective III	3
7.	EC655	HDL Programming Laboratory	2
Total			**23**

SEMESTER II

Sl. No.	Course Code	Course Title	Credits
1.	EC652	VLSI System Testing	4
2.	EC654	Electronic Design Automation Tools	4
3.	EC656	Design of ASICs	4
4.		Elective IV	3
5.		Elective V	3
6.		Elective VI	3
7.	EC658	Analog IC Design Laboratory	2
8.	EC660	ASIC – CAD Laboratory	2
Total			**25**

SUMMER TERM (Evaluation in Semester III)

Course Code	Course Title	Credits
EC699	Internship/Industrial Training/ Academic Attachment(I/A) (6 Weeks to 8 Weeks)	2
Total		**2**

SEMESTER III

Course Code	Course Title	Credits
EC697	PROJECT WORK - PHASE I	12
Total		**12**

SEMESTER IV

Course Code	Course Title	Credits
EC698	PROJECT WORK - PHASE II	12
Total		**12**

In addition to the Programme electives, students have to do 2 Open Electives offered by the institute or PG-level Online Courses from NPTEL (Can be completed from Semester I-IV) as given in the list. If students opt to do open electives from institute, they can choose open electives offered by MTech- Communication Systems or other departments.

Sl. No.	CODE	COURSE OF STUDY	C
1.		Open Elective I/Online Course I	3
2.		Open Elective II/Online Course II	3
		TOTAL OPEN ELCTIVE CREDITS	6

TOTAL CREDITS	
GRAND TOTAL	**23+25+2+12+12+6 = 80**

LIST OF ELECTIVES

Sl. No.	Course Code	Course Title	Credits
1.	MA617	Graph Theory and Discrete Optimization	3
2.	EC662	Modelling and Synthesis with Verilog HDL	3
3.	EC663	Optimizations of Digital Signal Processing Structures for VLSI	3
4.	EC664	Cognitive Radio	3
5.	EC665	VLSI Process Technology	3
6.	EC666	Analysis and Design of Digital Systems using VHDL	3
7.	EC667	Advanced Computer Architecture	3
8.	EC668	Low Power VLSI Systems	3
9.	EC669	VLSI Digital Signal Processing Systems	3
10.	EC670	Asynchronous System Design	3
11.	EC671	Advanced Digital Design	3
12.	EC672	Physical Design Automation	3
13.	EC673	Mixed - Signal Circuit Design	3
14.	EC674	Integrated Circuits for Wireless Communication	3
15.	EC675	Functional Verification using Hardware Verification Languages	3
16.	EC676	Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design	3
17.	EC677	High Speed System Design	3
18.	EC678	Modelling of Solid-State Devices	3
19.	EC679	Nano-Scale Devices: Modelling and circuits	3
20.	EC680	Embedded System Design	3
21.	EC681	Internet of Things	3
22.	EC682	Design and Testing of Advanced Semiconductor Memories	3
23.	EC683	FPGA Based System Design	3
24.	EC684	Bio-Medical CMOS ICs	3
25.	EC685	On-chip Antenna Design	3
26.	EC612	DSP Architecture	3
27.	EC613	High Speed Communication Networks	3
28.	EC615	Digital Image Processing	3

29.	EC616	RF MEMS	3
30.	EC626	Bio MEMS	3
31.	EC628	Pattern Recognition and Computational Intelligence	3
32.	EC632	Foundations of Artificial Intelligence	3
33.	EC635	Electromagnetic Interference and Compatibility	3
34.	EC636	Computer Vision	3
35.	EC637	Natural Language Processing	3
36.	EC638	Optimization Methods in Machine Learning	3
37.	EC639	Hardware for Deep Learning	3
38.	EC640	Image and Video Processing	3
39.	EC641	Automated Test Engineering for Electronics	3
40.	EC687	VLSI SoC Design and Verification	3
41.	EC688	VLSI Broadband Communication Circuits	3
42.	EC689	High Performance Frequency Synthesizers	3
43.	EC690	Analog Power Integrated Circuit Design	3

LIST OF NPTEL ONLINE COURSES

Sl. No.	Course Code	Course Title	Credits
1	EC801	Fundamentals of MIMO Wireless Communications	3
2	EC802	Evolution of Air Interface Towards 5G	3
3	EC803	Introduction to Industry 4.0 and Industrial Internet of Things	3
4	EC804	VLSI Data Conversion Circuits	3
5	EC805	Introduction to Time-Varying Electrical Networks	3
6	EC806	Power Management Integrated Circuits	3
7	EC807	Optical Wireless Communications beyond 5G Networks and IOT	3
8	EC808	5G Wireless Standard Design	3

LIST OF OPEN ELECTIVES (Offered to MTech Communication Systems and Other Branches)

Sl. No.	Course Code	Course Title	Credits
1.	EC701	Frequency Synthesizer Circuits	3
2.	EC702	Power Management Circuits	3

COURSE OUTCOME AND PO MAPPING PROGRAMME CORE Course Outcomes: On successful completion of the course, students will be able to:

Course Code	Course Name	CO	Course outcomes Students will be able to:	PO1	PO2	PO3
EC661	Digital System Design	CO1	Analyze algorithms and efficiently map them into hardware architectures.	3	1	2
		CO2	Analyze combinational network delays and power optimization techniques to optimize circuit speed and efficiency.	2	1	2
		CO3	Develop latch and flip-flop circuits tailored to specific design requirements.	3	1	2
		CO4	Develop and implement different data path modules and memory arrays for digital systems.	2	1	2
		CO5	Understand the principles of reconfigurable computing and its advantages over fixed architectures.	1	3	3
EC662	MODELING AND SYNTHESIS WITH VERILOG HDL	CO1	Understand the basic concepts of Verilog HDL	3	2	1
		CO2	Model digital systems in Verilog HDL at different levels of abstraction	3	3	1
		CO3	Know the simulation techniques and test bench creation	3	3	1
		CO4	Understand the design flow from simulation to synthesizable version	3	3	2
		CO5	Get an idea of the process of synthesis and post-synthesis	3	3	3
EC683	FPGA Based System Design	CO1	Create FPGA designs using HDLs, considering architectural constraints and efficiency.	3	2	1
		CO2	Develop DSP solutions, leveraging FPGA parallelism for real-time signal processing.	3	3	1
		CO3	Construct embedded systems with soft-core processors, enhancing customization capabilities.	3	3	1
		CO4	Optimize FPGA designs for timing, resource utilization, and power efficiency successfully.	3	3	2
		CO5	Evaluate and predict performance, demonstrating fault tolerance strategies competently.	3	3	3
EC663	Optimizations of Digital Signal Processing Structures for VLSI	CO1	understand the overview of DSP concepts and design architectures for DSP algorithms.	3	3	1
		CO2	improve the overall performance of DSP system through various transformation and optimization techniques.	2	3	2
		CO3	perform pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.	3	3	3
		CO4	Representation of a network of processing elements (PEs) that rhythmically compute and pass data through the system, and able to design basic arithmetic units and realize their architecture with higher radices	3	3	2

		CO5	understand clock-based issues, different clock styles and design asynchronous and wave pipelined systems.	3	3	2
EC669	VLSI Digital Signal Processing Systems	CO1	explain various transforms and their corresponding architectures, optimizing the design for computational complexity and speed.	3	2	1
		CO2	describe the knowledge of effect of round off noise computation	3	1	2
		CO3	design of both optimized Digital Lattice Filters	2	2	3
		CO4	design Bit level arithmetic Architectures and optimize the implementation of FIR filters and constant multipliers	3	2	2
		CO5	understand and create different numerical strength reduction techniques	2	3	3
EC652	VLSI System Testing	CO1	Analyse the concepts in testing which can help them design a better yield in IC design.	3	2	1
		CO2	Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.	3	2	1
		CO3	Describe the various test generation methods for static & dynamic CMOS circuits.	3	1	1
		CO4	Explain the design for testability methods for combinational & sequential CMOS circuits.	2	3	3
		CO5	Synthesize the BIST techniques for improving testability.	2	3	3
EC654	Electronic Design Automation Tools	CO1	Execute the special features of VLSI back end and front-end CAD tools and UNIX shell script	3	3	2
		CO2	Explain the algorithms used for ASIC construction	3	2	1
		CO3	Design synthesizable Verilog and VHDL code.	3	2	1
		CO4	Explain the difference between Verilog and system Verilog and are able to write system Verilog code.	3	2	1
		CO5	Model Analog and Mixed signal blocks using Verilog A and Verilog AMS	3	2	1
EC656	Designs of ASICs	CO1	Demonstrate VLSI tool-flow and appreciate FPGA and CPLD architectures.	3	2	2
		CO2	Understand the algorithms used for ASIC construction. Understand Full Custom Design Flow and Tool used.	2	3	3
		CO3	Understand Semicustom Design Flow and Tool used - from RTL to GDS and Logical to Physical Implementation.	3	3	2
		CO4	Understand about STA, LEC, DRC, LVS, DFM.	2	3	3
		CO5	Understand the System on Chip Design and On-chip communication architectures with case studies.	1	3	3

Course Code	**:**	**EC651**
Course Title	**:**	**Analog VLSI**
Number of Credits	**:**	**4**
Course Type	**:**	**Core**

CO5: appreciate the applications of graphs and digraphs in various other fields.

Course Learning Objectives

- To develop the ability to design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.
- To develop the skills to design analog VLSI circuits for a given specification.

Course Content

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.

Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch.

Text Books

1. *B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition 2016.*
2. *Paul. R.Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.*

Reference Books

1. *T. C. Carusone, D. A. Johns and K. Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.*
2. *P.E.Allen and D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.*
3. *R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.*
4. *Recent literature in Analog IC Design.*

Course outcomes

At the end of the course student will be able to

CO1: draw the equivalent circuits of MOS based Analog VLSI and analyse their performance.
CO2: design analog VLSI circuits for a given specification.
CO3: analyse the frequency response of the different configurations of an amplifier.
CO4: understand the feedback topologies involved in the amplifier design.
CO5: appreciate the design features of the differential amplifiers.

Course Code	**:**	**EC653**
Course Title	**:**	**Basics of VLSI**
Number of Credits	**:**	**4**
Course Type	**:**	**Core**

Course Learning Objectives

- To provide rigorous foundation in MOS and CMOS digital circuits
- To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity

Course Content

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops, CMOS fabrication and layout, VLSI design flow.

MOS transistor theory: Ideal I-V and C-V characteristics, non-ideal I-V effects, DC transfer characteristics, Switch level RC delay models.

CMOS technologies: Layout design rules, CMOS process enhancement, Technology related CAD issues.

Circuit characterization and performance estimation: Delay estimation, Logical effort and transistor sizing, Power dissipation, Interconnect design margin, Reliability, Scaling.

Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits.

Text Books

1. *N.H.E.Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2011.*
2. *J.Rabey and B. Nikolic, "Digital Integrated circuits", 2nd Edition, Pearson, 2003.*

Reference Books

1. *Pucknell and Eshraghian, "Basic VLSI Design", 3rd Edition, PHI, 1996.*
2. *Recent literature in Basics of VLSI.*

Course outcomes

At the end of the course student will be able to
CO1: implement the logic circuits using MOS and CMOS technology.
CO2: analyse various circuit configurations and their applications
CO3: analyse the merits of circuits according to the technology and applications change.
CO4: design low power CMOS VLSI circuits.
CO5: understand the rapid advances in CMOS Technology

Course Code	**:**	**EC661**
Course Title	**:**	**Digital System Design**
Number of Credits	**:**	**4**
Course Type	**:**	**Core**

Course Learning Objective

- To get an idea about designing complex, high speed digital systems and how to implement such design.

Course Content

Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.

Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architectures- Single context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

Text Books

1. *N.H.E.Weste, D. Harris, "CMOS VLSI Design, 4th Edition", Pearson, 2010.*
2. *W.Wolf, "FPGA- based System Design", Pearson, 2004.*
3. *S.Hauck and A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008.*

Reference Books

1. *F.P. Prosser and D. E. Winkel, "Art of Digital Design", 1987.*
2. *R.F.Tinde, "Engineering Digital Design", 2nd Edition, Academic Press, 2000.*
3. *C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.*
4. *M.Gokhale and P.S.Graham, "Reconfigurable computing: accelerating computation with field-programmable gate arrays", Springer, 2005.*
5. *C.Roth, "Fundamentals of Digital Logic Design", Jaico Publishers, 5th Edition, 2009.*
6. *Recent literature in Digital System Design.*

Course outcomes

At the end of the course student will be able to

CO1: identify mapping algorithms into architectures.
CO2: summarize various delays in combinational circuit and its optimization methods.
CO3: summarize circuit design of latches and flip-flops.
CO4: construct combinational and sequential circuits of medium complexity that is based on VLSIs, and programmable logic devices.
CO5: summarize the advanced topics such as reconfigurable computing, partially reconfigurable, Pipeline reconfigurable architectures and block configurable.

Course Code	**:**	**EC655**
Course Title	**:**	**HDL Programming Laboratory**
Number of Credits	**:**	**2**
Course Type	**:**	**Laboratory**

List of Experiments

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flip flop
6. Shift Register/ Universal Shift Register
7. Comparator
8. Up counter/ Down counter
9. Udps
10. Memory – ROM, RAM
11. Array Multiplier/ Array Multiplier With Pipelining
12. Fir Filter/ Fir Filter With Pipelining

List of Experiments

1. Design of 8-bit Carry Skip Adder and Carry Save Adder
2. Design of 4-bit Array Multiplier with and without Pipelining
3. Design of 4-tap FIR Filter with and without Pipelining
4. Design of FIFO
5. Design of Sequence Detector
6. Design of 8-bit ALU
7. Project: Design of 16-point FFT

Course outcomes:

After successful completion of the laboratory course, the students are able to

CO1: to learn the basic HDL functions

CO2: Design and analyse the combinational and sequential circuits using Verilog HDL tools.

CO3: Perform FPGA Implementation for Verilog HDL designs on development board

CO4: Implement FIR algorithms in FPGA

CO5: Implement FFT algorithm in FPGA

Course Code	**:**	**EC652**
Course Title	**:**	**VLSI System Testing**
Number of Credits	**:**	**4**
Course Type	**:**	**Core**

Course Learning Objective

- To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

Course Content

Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing: Memory fault models, Classical Test Algorithms, Memory Fault simulation.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books

1. *N. Jha and S.D. Gupta, "Testing of Digital Systems", Cambridge, 2003.*
2. *W. W. Wen, "VLSI Test Principles and Architectures Design for Testability", Morgan Kaufmann Publishers. 2006.*

Reference Books

1. *Michael L. Bushnell and Vishwani D. Agrawal," Essentials of Electronic Testing for Digital, memory and Mixed signal VLSI Circuits", Kluwar Academic Publishers. 2000.*
2. *P. K. Lala, "Digital circuit Testing and Testability", Academic Press. 1997.*
3. *M. Abramovici, M. A. Breuer, and A.D. Friedman, "Digital System Testing and Testable Design", Computer Science Press, 1990.*
4. *Recent literature in VLSI System Testing.*

Course outcomes

At the end of the course student will be able to

CO1: apply the concepts in testing which can help them design a better yield in IC design.

CO2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.

CO3: analyse the various test generation methods for static and dynamic CMOS circuits.

CO4: identify the design for testability methods for combinational and sequential CMOS circuits.

CO5: recognize the BIST techniques for improving testability.

Course Code	**:**	**EC654**
Course Title	**:**	**Electronic Design Automation Tools**
Number of Credits	**:**	**4**
Course Type	**:**	**Core**

Course Learning Objective

- To make the students exposed to Front end and Back end VLSI CAD tools.

Course Content

OS Architecture: System settings and configuration. Introduction to UNIX commandsHandling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection. Working on Vi editor, Basic Shell Programming, TCL Scripting language.

Circuit simulation using Spice - circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and OpAmp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

Synthesis and simulation using HDLs-Logic synthesis using Verilog. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

System Verilog- Introduction, Design hierarchy, Data types, Operators and language constructs. Functional coverage, Assertions, Interfaces and test bench structures.
Analog/Mixed Signal Modelling and Verification: Analog/Mixed signal modelling using Verilog-A and Verilog-AMS. Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling using Verilog-RNM/System Verilog. Analog/Digital Boundary Issues: boundary issues coverage. Introduction to Universal Verification Methodology (UVM).

Text Books

1. *M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2008.*
2. *M.H.Rashid, "Spice for Circuits and Electronics using Pspice", 2nd Edition, PHI.*
3. *S.Sutherland, S. Davidmann and P. Flake, "System Verilog for Design", 2nd Edition, Springer, 2006.*

Reference Books

1. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*
2. *Z. Dr Mark, "Digital System Design with System Verilog", Pearson, 2010.*
3. *Sharon Rosenberg and Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", 2nd edition, 2010.*

Course outcomes

After successful completion of the course the students are able to
CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script
CO2: write Pspice code for any electronics circuit and to perform monte-carlo analysis and sensitivity/worst case analysis.
CO3: design synthesizable Verilog and VHDL code.
CO4: explain the difference between Verilog and system Verilog and are able to write system Verilog code.
CO5: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS.

Course Code	**:**	**EC656**
Course Title	**:**	**Design of ASICs**
Number of Credits	**:**	**4**
Course Type	**:**	**Core**

Course Learning Objectives

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and Platform based design.
- To give the student an understanding of High performance algorithms.

Course Content

Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs – Anti-fuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors. Self-Study: Multi-core processors, High performance computing (HPC), Cache, High speed memories (DDR4), High speed serdes (56Gbps, PAM4), GPU, High performance algorithms for ASICs/ SoCs, FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs.

ASIC physical design issues, System Partitioning, Floor planning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs and Applications. Schematicand layout basics, Full Custom Design Flow.

Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation.

Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM. System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. **Case study:** FSM design, clock domain crossing, FIFOs. Core (ARM) and IOs (I2C, PWM, GPIO, SPI, NAND, Ethernet, USB, high speed serdes etc. are interconnected through AXI/APB buses (protocols and interconnects)

Text Books

1. *M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2003.*
2. *Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier, 2008.*

Reference Books

1. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*
2. *Jan.M.Rabaey et al, "Digital Integrated Circuit Design Perspective", 2nd Edition, PHI 2003.*
3. *David A.Hodges, "Analysis and Design of Digital Integrated Circuits", 3rd Edition, MGH 2004.*
4. *Hoi-Jun Yoo, Kangmin Lee and Jun Kyong Kim, "Low-Power NoC for High-Performance SoC Design", CRC Press, 2008.*
5. *"An Integrated Formal Verification solution DSM sign-off market trends", www.cadence.com.*
6. *Recent literature in Design of ASICs.*

Course outcomes

At the end of the course student will be able to

CO1: explain VLSI tool-flow and appreciate FPGA architecture.

CO2: describe the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.

CO3: explain the algorithms used for ASIC construction

CO4: analyse the basics of System on Chip, On chip communication architectures like AMBA, AXI and utilizing Platform based design.

CO5: synthesize high performance algorithms available for ASICs

Course Code	**:**	**EC658**
Course Title	**:**	**Analog IC Design Laboratory**
Number of Credits	**:**	**2**
Course Type	**:**	**Laboratory**

List of Experiments

1. Characteristics of NMOS and PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Common Gate Amplifier
4. Design of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Opamp
9. Design of Telescopic Cascode Opamp
10. Design of Folded Cascode Opamp

Course outcomes

After successful completion of the laboratory course, the students are able to

CO1: Introduce industry standard Analog IC design EDA tool

CO2: Practical learning and understanding of Analog amplifiers, current mirrors etc.

CO3: Solve analog design problems by changing the design parameter of the circuit with the help of Cadence Virtuoso.

CO4: understand the working of circuits and enhance the analog design skills.

CO5: Learn the art of analog layout in IC design.

Course Code	**:**	**EC660**
Course Title	**:**	**ASIC – CAD Laboratory**
Number of Credits	**:**	**2**
Course Type	**:**	**Laboratory**

List of Experiments

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. MAC
7. Memory

The above experiments are carried out using the following tools:

1. Model SIM
2. Cadence
3. Synopsis
4. Mentor Graphics
5. Xilinx Plan ahead

List of Experiments

1. Design of MOD 10 Counter using Verilog
2. Design of MAC Unit using Verilog
3. Design of 8 bit Signed Booth Multiplier using Verilog
4. Design of 4 tap FIR Filter using Verilog
5. Design of Address Generator block for WiMAX Interleaver using Verilog
6. Project: Design of Vending Machine Block using Verilog

The above experiments are carried out using the following tools:

1. Xilinx ISE Design Suite
2. Cadence
3. Synopsis

Course outcomes:

After successful completion of the laboratory course, the students are

CO1: Familiar with sophisticated VLSI CAD tools available in the lab.

CO2: Able to design and implement any ASIC designs using the latest VLSI CAD tools.

CO3: Perform full custom ASIC design of digital blocks

CO4: Learn advanced features in physical design

CO5: Complete cycle from design to chip tape-out procedure

Course Code	**:**	**MA617**
Course Title	**:**	**Graph Theory and Discrete Optimization**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To have general awareness of some application oriented concepts in discrete structures and apply them as a tool in the problems related to general communication network.

Course Content

Basic definitions, examples and some results, relating degree, walk, trail, path, tour, cycle, complement of a graph, self-complementary graph, Connectedness, Connectivity, distance, shortest path, radius, diameter and Bipartite graphs. Some eccentric properties of graphs, tree, spanning tree, coding of spanning tree. Number of spanning trees in a complete graph. Recursive procedure to find number of spanning trees. Construction of spanning trees.

Directed graphs: some standard definitions and examples of strongly, weakly, unilaterally connected digraphs, strong components and deadlock. Matrix representation of graph and digraphs. Some properties (proof not expected). Eulerian graphs and standard results relating to characterization of Eulerian graphs. Hamiltonian graph-standard theorems (Dirac theorem, Chavtal theorem, closure of graph). Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems.

Chromatic number; vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity, Five colour theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.

Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs.

DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.

Text Books

1. *J.A. Bondy and U.S.R.Murthy, "Graph Theory with Applications", Macmillan, London, 1976, EBook, Freely Downloadable.*
2. *Cormen, Leiserson, Rivest and Stein, "Introduction to Algorithms", 2nd Edition, McGraw-Hill, 2001.*

Reference Books

1. *M.Gondran and M.Minoux, "Graphs and Algorithms", John Wiley, 1984.*
2. *H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999.*

Course outcomes

At the end of the course student will be able to

CO1: understand the various types of graphs, graph properties and give examples for the given property

CO2: model the given problem from their field to underlying graph model.

CO3: proceed to solve the problem either through approximation algorithm or exact algorithm depending on the problem nature.

CO4: appreciate the applications of digraphs and graphs in various communication networks.

Course Code	**:**	**EC662**
Course Title	**:**	**Modeling and Synthesis with Verilog HDL**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioural and RTL modelling of digital circuits
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools
- To simulate, synthesize, and program their designs on a development board
- To verify and design the digital circuit by means of Computer Aided Engineering tools which involves in programming with the help of Verilog HDL.

Course Content

Hardware modeling with the verilog HDL. Encapsulation, modeling primitives, different types of description.

Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection. Delay simulation in Verilog and FPGA implementation.

Behavioral descriptions in Verilog HDL. Synthesis of combinational logic. FPGA Implementation

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines on FPGA, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in Verilog and Implementation on FPGA.

Text Books

1. *M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", PHI, 1999.*
2. *S. Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", Pearson, 2003.*

Reference Books

1. *J Bhaskar, "A Verilog HDL Primer", 3rd Edition, Kluwer, 2005.*
2. *M.G.Arnold, "Verilog Digital – Computer Design", Prentice Hall (PTR), 1999.*
3. *Recent literature in Modeling and Synthesis with Verilog HDL.*

Course outcomes

At the end of the course student will be able to
CO1: understand the basic concepts of verilog HDL
CO2: model digital systems in verilog HDL at different levels of abstraction
CO3: know the simulation techniques and test bench creation.
CO4: understand the design flow from simulation to synthesizable version
CO5: get an idea of the process of synthesis and post-synthesis

Course Code	**:**	**EC663**
Course Title	**:**	**Optimizations of Digital Signal Processing Structures for VLSI**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To enable students to develop a practical understanding of VLSI implementing DSP algorithms with optimized hardware.
- To enable students to design filters with high speed and low power using pipelining methodologies
- To understand Systolic Architecture designs and efficient date driven architectures for DSP applications
- To encourage students to know the limitations of synchronous designs and exploration of Asynchronous design techniques

Course Content

An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.

Transformation Techniques: Iteration bound, Retiming, Folding and Unfolding

Pipeline interleaving in digital filters. Pipelining and Parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Systolic Architecture Design: Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector. Redundant arithmetic: Redundant Number Representations, Carry-Free Radix-2 addition and subtraction, Hybrid radix-4 addition, Radix-2 hybrid redundant multiplication architectures.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems, Asynchronous pipelining.

Text Book*:*

1. *K.K.Parhi, VLSI Digital Signal Processing Systems, John-Wiley, reprint 2011.*

Reference Books*:*

1. *FPGA-based Implementation of Signal Processing Systems, 2nd Edition by Roger Woods et al., 2017*
2. *Digital Signal Processing with Field Programmable Gate Arrays by Uwe Meyer-Baese, reprint 2007*
3. *Magdy A. Bayoumi, VLSI Design Methodologies for Digital Signal Processing, 2012*
4. *VLSI Design Methodologies for Digital Signal Processing Architectures by Parhi and Nishitan, First Edition, 2005*
5. *VLSI Signal Processing Technology edited by Magdy A. Bayoumi and Earl E. Swartzlander, , First Edition, 2012*

Course outcomes

At the end of the course student will be able to

CO1: understand the overview of DSP concepts and design architectures for DSP algorithms.
CO2: improve the overall performance of DSP system through various transformation and optimization techniques.
CO3: perform pipelining and parallel processing on FIR and IIR systems to achieve high speed and low power.
CO4: Representation of a network of processing elements (PEs) that rhythmically compute and pass data through the system, and able to design basic arithmetic units and realize their architecture with higher radices
CO5: understand clock-based issues, different clock styles and design asynchronous and wave pipelined systems.

Course Code	**:**	**EC664**
Course Title	**:**	**Cognitive Radio**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- This subject introduces the fundamentals of multi rate signal processing and cognitive radio.

Course Content

Filter banks-uniform filter bank. Direct and DFT approaches. Introduction to ADSL Modem. Discrete multi-tone modulation and its realization using DFT. QMF. STFT. Computation of DWT using filter banks.

DDFS- ROM LUT approach. Spurious signals, jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC.CORDIC architectures.

Block diagram of a software radio. Digital down converters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS. Down conversion using discrete Hilbert transform. Under sampling receivers, Coherent demodulation schemes.

Concept of Cognitive Radio, Benefits of Using SDR, Problems Faced by SDR, Cognitive Networks, Cognitive Radio Architecture. Cognitive Radio Design, Cognitive Engine Design.

A Basic OFDM System Model, OFDM based cognitive radio, Cognitive OFDM Systems, MIMO channel estimation, Multi-band OFDM, MIMO-OFDM synchronization and frequency offset estimation. Spectrum sensing to detect Specific Primary System, Spectrum Sensing for Cognitive OFDMA Systems.

Text Books

1. *U. Meyer – Baese, "Digital Signal Processing with FPGAs", Springer, 2004.*
2. *H. Arslan "Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems", University of South Florida, USA, Springer, 2007.*
3. *J. H. Reed, "Software Radio: A modern Approach to Radio Design", Pearson, 2002.*

Reference Books

1. *S. K. Mitra, "Digital Signal processing", Mc GrawHill, 1998*
2. *K.C.Chen and R.Prasad, "Cognitive Radio Networks", Wiley, 2009-06-15.*
3. *T. W. Rondeau, C.W.Bostian, "Artificial Intelligence in Wireless Communications", 2009.*
4. *Tusi, "Digital Techniques for Wideband receivers", Artech House, 2001.*
5. *T. DarcChiueh and P. Yun Tsai, "OFDM baseband receiver design for wireless communications", Wiley, 2007*
6. *Jerry R. Hampton, "Introduction to MIMO Communications", Cambridge University Press 2014.*
7. *Recent literature in Cognitive Radio.*

Course outcomes

At the end of the course student will be able to

CO1: gain knowledge on multirate systems.

CO2: develop the ability to analyze, design, and implement any application using FPGA.

CO3: be aware of how signal processing concepts can be used for efficient FPGA based system design.

CO4: understand the rapid advances in Cognitive radio technologies.

CO5: explore DDFS, CORDIC and its application.

Course Code	**:**	**EC665**
Course Title	**:**	**VLSI Process Technology**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To provide rigorous foundation in MOS and CMOS fabrication process.

Course Content

Electron grade silicon. Crystal growth. Wafer preparation. Vapour phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.

Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.

Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

Analytical and assembly techniques. Packaging of VLSI devices.

Text Books

1. *S.M.Sze, "VLSI Technology", 2nd Edition , McGraw Hill, 1988*
2. *W. Wolf, "Modern VLSI Design", 3rd Edition, Pearson,2002*

Reference Books

1. *James D. Plummer, "Silicon VLSI Technology: Fundamentals, Practice and Modelling", Pearson Education, 2000*
2. *Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", 2nd Edition, Oxford University Press 2001*
3. *C.Y. Chang and S.M.Sze, "ULSI Technology", McGraw Hill ,1996.*

Course outcomes

At the end of the course student will be able to
CO1: appreciate the various techniques involved in the VLSI fabrication process.
CO2: understand the different lithography methods and etching process.
CO3: appreciate the deposition and diffusion mechanisms.
CO4: analyze the fabrication of NMOS, CMOS memory and bipolar devices
CO5: understand the nuances of assembly and packaging of VLSI devices.

Course Code	**:**	**EC666**
Course Title	**:**	**Analysis and Design of Digital Systems using VHDL**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To prepare the student to understand the VHDL language feature to realize the complex digital systems.
- To design and simulate sequential and concurrent techniques in VHDL
- To explain modeling of digital systems using VHDL and design methodology
- To explain predefined attributes and configurations of VHDL.
- To Understand behavioral, non-synthesizable VHDL and its role in modern design

Course Content

An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL. Basic concepts and structural descriptions in VHDL.

Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments. Structural specification of hardware.

Design organization, parameterization and high level utilities, definition and usage of subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries. Utilities for high-level descriptions.

Data flow and behavioural description in VHDL- multiplexing and data selection, state machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities. Behavioural description of hardware.

CPU modelling for discrete design- Parwan CPU, behavioural description, bussing structure, data flow, test bench, a more realistic Parwan. Interface design and modelling. VHDL as a modelling language.

Text Books

1. *Z.Navabi, "VHDL Analysis and Modelling of Digital Systems", 2nd Edition, McGraw Hill, 1998.*
2. *Perry, "VHDL", 3rd Edition, McGraw Hill.2002*

Reference Books

1. *A. Dewey, "Analysis and Design of Digital Systems with VHDL", CL-Engineering, 1996.*
2. *Z.Navabi, "VHDL: modular design and synthesis of cores and systems", McGraw Hill, 2007.*
3. *C. H. Roth, Jr., L.K.John, "Digital Systems Design Using VHDL" Thomson Learning EMEA Limited, 2008.*
4. *Recent literature in Analysis and Design of Digital Systems using VHDL.*

Course outcomes

At the end of the course student will be able to

CO1: model, simulate, verify, and synthesize with hardware description languages.
CO2: understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements.
CO3: design digital logic circuits in different types of modelling.
CO4: demonstrate timing and resource usage associated with modelling approach.
CO5: use computer-aided design tools for design of complex digital logic circuits.

Course Code	**:**	**EC667**
Course Title	**:**	**Advanced Computer Architecture**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To give an exposure on look ahead pipelining- parallelism, multiprocessor scheduling, multithreading and various memory organizations.

Course Content

Multiprocessors and multi-computers. Multi-vector and SIMD computers. PRAM and VLSI Models. Conditions of parallelism. Program partitioning and scheduling. Program flow mechanisms. Parallel processing applications. Speed up performance law.

Advanced processor technology. Superscalar and vector processors. Memory hierarchy technology. Virtual memory technology. Cache memory organization. Shared memory organization.

Linear pipeline processors. Non linear pipeline processors. Instruction pipeline design. Arithmetic design. Superscalar and super pipeline design. Multiprocessor system interconnects. Message passing mechanisms.

Vector Processing principle. Multivector multiprocessors. Compound Vector processing. Principles of multithreading. Fine grain multicomputer. Scalable and multithread architectures. Dataflow and hybrid architectures.

Parallel programming models. Parallel languages and compilers. Parallel programming environments. Synchronization and multiprocessing modes. Message passing program development. Mapping programs onto multicomputer. Multiprocessor UNIX design goals. MACH/OS kernel architecture. OSF/1 architecture and applications.

Text Books

1. *K. Hwang, "Advanced Computer Architecture", Tata McGraw Hill, 2016.*
2. *W. Stallings, "Computer Organization and Architecture", McMillan, 2012.*

Reference Book

1. *M.J. Quinn, "Designing Efficient Algorithms for Parallel Computer", McGraw Hill, 1994.*
2. *Recent literature in Advanced Computer Architecture.*

Course outcomes

At the end of the course student will be able to
CO1: apply the basic knowledge of partitioning and scheduling in Multiprocessors.
CO2: analyze and design cache memory, virtual memory and shared memory organizations.
CO3: distinguish and analyze the design properties of Linear and Non - Linear processors.
CO4: analyze the principles of multithreading in hybrid Architectures.
CO5: write any parallel programming models for various architectures and Applications.

Course Code	**:**	**EC668**
Course Title	**:**	**Low Power VLSI Systems**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To expose the students to the low voltage device modeling, low voltage, low power VLSI CMOS circuit and system design.

Course Content

Evolution of CMOS technology, CMOS fabrication process, shallow trench isolation, Lightly-doped drain, Buried channel. Bi-CMOS and SOI CMOS technologies, second order effects, Modeling of MOS devices, Threshold voltage, Body effect, Short channel and Narrow channel effects, Electron temperature, MOS capacitance.

CMOS inverters, Differential static logic circuits, Pass transistor, Bi-CMOS, SOI CMOS, Low voltage and low power CMOS static logic circuit design techniques.

Basic concepts of dynamic logic circuits. Charge sharing, Noise and race problems, NORA, Zipper, Domino, Dynamic differential, BiCMOS, low voltage and low power dynamic logic techniques.

CMOS memory circuits, SRAM, DRAM, Bi-CMOS and Nonvolatile memory circuits.

Basics of clock gating and power gating. Key characteristics of the Unified Power Format (UPF) in low power design. CMOS VLSI systems, Adder circuits, Multipliers and advanced structures – PLA, PLL, DLL and processing unit.

Text Books

1. *J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems", Springer, 2009*
2. *J.B.KuoandJ.H.Lou, "Low-voltage CMOS VLSI Circuits", Wiley, 1999.*

Reference Books

1. *Michael Keating etal. "Low Power Methodology Manual For System-on-Chip Design" Springer, 2008*
2. *A.Bellaowar and M.I.Elmasry, "Low power Digital VLSI Design, Circuits and Systems", Kluwer, 1996.*
3. *IEEE Standard for Design and Verification of Low-Power, Energy- Aware Electronic Systems Sponsored by the Design Automation Standards Committee, IEEE Computer Society, 2015*

Course outcomes

At the end of the course student will be able to

CO1: acquire the knowledge about various CMOS fabrication process and its modelling and infer about the second order effects of MOS transistor characteristics.
CO2: analyze and implement various CMOS low voltage and low power static logic circuits.
CO3: learn the design of various CMOS low voltage and low power dynamic logic circuits.
CO4: learn the different types of memory circuits and their design.
CO5: design and implementation of various structures for low power applications.

Course Code	**:**	**EC669**
Course Title	**:**	**VLSI Digital Signal Processing Systems**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand the various VLSI architectures for digital signal processing and convolutional algorithms
- To know the Numerical strength reductions and algorithmic strength reduction in the filter structures.
- To understand scaling and Round-off Noise effects in DSP systems.
- To develop bit-level arithmetic units to implement DSP algorithms.

Course Content

An overview of DSP concepts, Representations of DSP algorithms. Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

Scaling and Round off Noise - State variable description of digital filters, Scaling and Round off Noise computation, Round off Noise in Pipelined IIR Filters, Round off Noise Computation using state variable description, Slow-down, Retiming and Pipelining.

Digital Lattice Filter Structures: Schur Algorithm, Derivation of One-Multiplier Lattice Filter, Normalized Lattice Filter, Pipelining of Lattice Filter.

Bit level arithmetic Architectures- parallel multipliers, interleaved floor-plan and bit-plane-based digital filters, Bit serial multipliers, Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

Numerical Strength Reduction - Subexpression Elimination, Multiple Constant Multiplication, Subexpression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

Text Book

1. *K.K.Parhi, "VLSI Digital Signal Processing Systems", John-Wiley, 2007.*

Reference Book

1. *FPGA-based Implementation of Signal Processing Systems, 2nd Edition by Roger Woods et al., 2017*
2. *Digital Signal Processing with Field Programmable Gate Arrays by Uwe Meyer-Baese, reprint 2007*
3. *Magdy A. Bayoumi, VLSI Design Methodologies for Digital Signal Processing, 2012*
4. *VLSI Design Methodologies for Digital Signal Processing Architectures by Parhi and Nishitan, First Edition, 2005*
5. *VLSI Signal Processing Technology edited by Magdy A. Bayoumi and Earl E. Swartzlander, , First Edition, 2012*

Course outcomes

At the end of the course student will be able to

CO1: explain various transforms and their corresponding architectures, optimizing the design for computational complexity and speed.

CO2: describe the knowledge of effect of round off noise computation

CO3: design of both optimized Digital Lattice Filters

CO4: design Bit level arithmetic Architectures and optimize the implementation of FIR filters and constant multipliers

CO5: understand and create different numerical strength reduction techniques

Course Code	**:**	**EC670**
Course Title	**:**	**Asynchronous System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- This subject introduces the fundamentals and performance of Asynchronous system
- To familiarize the dependency graphical analysis of signal transmission graphs
- To learn software languages and its syntax and operations for implementing Asynchronous Designs

Course Content

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

Speed-independent control circuits: Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, more advanced latch control circuits.

High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

Text Books

1. *Chris. J. Myers, "Asynchronous Circuit Design", John Wiley and Sons, 2001.*
2. *Kees Van Berkel, "Handshake Circuits An Asynchronous architecture for VLSI programming" Cambridge University Press, 2004*

Reference Books

1. *Jens Sparso, Steve Furber, "Principles of Asynchronous Circuit Design", Kluwer Academic Publishers, 2001.*
2. *Richard F. Tinder, "Asynchronous Sequential Machine Design and Analysis", Morgan and Claypool Publishers, 2009*
3. *Peter A. Beerel, Recep O. Ozdag, Marcos Ferretti, "A Designer's Guide to Asynchronous VLSI", Cambridge University Press, 1st Edition, 2010*
4. *Recent literature in Asynchronous System Design.*

Course outcomes

At the end of the course student will be able to
CO1: understand the fundamentals of Asynchronous protocols
CO2: analyse the performance of Asynchronous System and implement handshake circuits
CO3: understand the various control circuits and Asynchronous system modules
CO4: gain the experience in using high level languages and tools for Asynchronous Design
CO5: learn commands and control flow of Balsa language for implementing Asynchronous Designs

Course Code	**:**	**EC671**
Course Title	**:**	**Advanced Digital Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To make the students learn about graphical models and state diagram in designing optimized digital circuits.
- To provide the students a detailed knowledge of scheduling algorithm, synthesis of pipelined circuits and scheduling pipelined circuits
- To enable the students to design digital design with advanced technique like Sequential logic optimization and test the designed circuit Testability considerations.

Course Content

Different types of graphs. Combinational optimization- Graph optimization problems and algorithms. Boolean functions, statisfiability and cover. Abstract models, state diagrams. Data flow and sequencing graphs, compilation and behavioural optimization.

Architectural synthesis - Circuit specifications for architectural synthesis. Temporal domain, spatial domain, hierarchical models. Synchronization problems. Area and performance estimation. Strategies for architectural optimization, Data path synthesis of pipelined circuits.
Scheduling algorithms-Scheduling with and without constraints. Scheduling algorithms for extended sequencing models. Scheduling pipelined circuits.

Resource sharing and binding. Sharing and binding for resource dominated circuits and general circuits. Concurrent binding and scheduling. Resource sharing and binding for non-scheduled sequencing graphs.

Sequential logic optimization-sequential circuit optimization using state based models and network models. Implicit finite state machine. Traversal methods. Testability considerations for synchronous circuits.

Text Books

1. *G.De Micheli, "Synthesis and optimization of Digital circuits", McGraw Hill, 1994* .
2. *C. Roth, "Fundamentals of Digital Logic Design", Jaico Publishers, V ed., 2009.*
3. *Balabanian, "Digital Logic Design Principles", Wiley publication, 2007.*

Reference Books

1. *J. F. Wakerly, "Digital Design principles and practices", 3rd Edition, PHI publication, 1999.*
2. *S.Brown, "Fundamentals of digital logic", Tata McGraw Hill publication, 2007.*
3. *N. N. Biswas, "Logic Design Theory", Prentice Hall of India, 2001.*
4. *John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2006.*
5. *Recent literature in Advanced Digital Design.*

Course outcomes

At the end of the course student will be able to
CO1: understand advanced state of art techniques of digital design.
CO2: synthesis the circuits and evaluate its performance in terms of area, power and speed.
CO3: understand the use of scheduling algorithm.
CO4: gain in-depth knowledge of sequential digital circuits designed using resource sharing.
CO5: understand synchronization across clock domains, timing analysis, and Testability considerations

Course Code	**:**	**EC672**
Course Title	**:**	**Physical Design Automation**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods

Course Content

VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Text Books

1. *S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley (India), 2006.*
2. *N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer, 2012.*

Reference Books

1. *S.M. Sait, H. Youssef, "VLSI Physical Design Automation", Cambridge India, 2010.*
2. *M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.*
3. *Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw Hill, 2017.*
4. *Andrew B. Kahng and Jens Lienig "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011.*
5. *Recent literature in Physical Design Automation.*

Course outcomes

At the end of the course student will be able to

CO1: Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.

CO2: Students are able to solve the performance issues in circuit layout.

CO3: Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing

CO4: Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing

CO5: Students are able to analyze circuits using both analytical and CAD tools

Course Code	**:**	**EC673**
Course Title	**:**	**Mixed - Signal Circuit Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To make the students to understand the design and performance measures concept of mixed signal circuit.

Course Content

Concepts of Mixed-Signal Design and Performance Measures. Introduction and Principle behind ADC's and DAC's - Performance Metrics of ADCs and DACs, Nyquist Rate DACs, Comparators-Characterization – Two stage comparators – open loop comparators, Nyquist rate ADCs: Flash, SAR, Pipelined, Time-interleaved ADCs. Overview of oversampling ADCs.

Design methodology for mixed signal IC design using gm/Id concept.

Design of Current mirrors. References. Comparators and Operational Amplifiers.

CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

Design of frequency and Q tunable continuous time filters.

Text Books

1. *David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 1997.*
2. *B. Razavi, "Principles of Data Conversion System Design", Wiley-IEEE Press, 1St Edition, 1994.*
3. *R. J. Baker, "CMOS Mixed Signal circuit Design", Wiley-IEEE Press, 2nd Edition, 2008.*
4. *M.Gustavsson, J. J. Wikner, and N. N. Tan, "CMOS Data Conversion for Communications", Springer; 2000*

Course outcomes

At the end of the course student will be able to
CO1: appreciate the fundamentals of data converters and also optimized their performances.
CO2: understand the design methodology for mixed signal IC design using gm/Id concept.
CO3: analyze the design of current mirrors and operational amplifiers
CO4: design the CMOS digital circuits and implement its layout.
CO5: design the frequency and Q-tunable time domain filters.

Course Code	**:**	**EC674**
Course Title	**:**	**Integrated Circuits for Wireless Communication**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To impart knowledge on basics of CMOS IC design at RF frequencies.
- To be familiar with the circuits used in RF front end in transceiver design.

Course Content

Overview of RF systems: wireless transmitter and receiver architectures. Characteristics of passive IC components at RF frequencies - interconnects, resistors, capacitors, inductors and transformers - transmission lines. Effects of non-linearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded non-linear stages, and AM/PMconversion. Noise - classical two-port noise theory, representation of noise in circuits. Narrowband and wideband amplifiers - bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and uni-lateralization concepts.

Low noise amplifier (LNA) design, Friis'equation, input matching, common source LNA with inductive load, resistive feedback, and inductive degeneration topologies, common gate LNA topologies, noise cancelling and reactance cancelling LNA, high IP2 differential LNA.

Mixer circuits performance parameters (gain, noise figure, input impedance, and LO self mixing), passive and active down-conversion mixers, active mixers with current source helpers, high IP2, low flicker noise, and high transconductance performance metrics. Up-conversion mixers.

Single ended and differential PA's, efficiency and linearity metrics, Class A, AB, B, C, D, E and F amplifiers, modulation in power amplifiers, linearity enhancement techniques, and design examples.

Transceiver design system level considerations such as Rx noise figure and non-linearity, variable gain amplifier (VGA) range, Tx output power, phase noise, and frequency planning. Design of receiver circuits- LNA, mixer, and VGA, and transmitter circuits - PA, up-converter, and frequency synthesizer. Case studies from IEEExplore. RFIC simulation and layout- general layout issues, passive and active component layout.

Text Books

1. *Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd Edition, Cambridge University Press, 2004.*
2. *B. Razavi, "RF Microelectronics", 2nd Edition, Prentice Hall, 1998.*

Reference Books

1. *A. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 1999.*
2. *R. Ludwig and P. Bretchko, "RF Circuit Design, Theory and Applications", Pearson, 2000.*
3. *Mattuck,A., "Introduction to Analysis", Prentice-Hall,1998.*

Course outcomes

At the end of the course student will be able to
CO1: understand the basics of RF system design and analyse the high frequency amplifier design
CO2: appreciate the need for LNA and learn different LNA topologies and design techniques
CO3: understand the requirement of RF Mixer, its function and performance parameters
CO4: analyse the various types of synthesizers, oscillators and their characteristics.
CO5: learn about the need for power amplifiers and the effects of nonlinearities

Course Code	**:**	**EC675**
Course Title	**:**	**Functional Verification using Hardware Verification Languages**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To expose the students to all aspects of functional verification of digital systems

Course Content

System Verilog (SV) - Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks and Functions, Procedural Statements, Interfaces, Basic OOPs, Randomization, Threads and Inter Process Communication, Advanced OOPs and Test bench guidelines, Advanced Interfaces.

A Complete System Verilog Test Bench (SVTB), Functional Coverage in System Verilog, Interfacing with C, FSM Modelling with SV, Connecting Test bench and Design, Behavioral and Transaction Level Modelling with SV

System Verilog Assertions (SVA) – Introduction to SVA, Building blocks, Properties, Boolean expressions, Sequence, Single and Multiple Clock definitions, Implication operators (Overlapping and Non-overlapping), Repetition operators, Built-in System functions ($past, $stable, $onehot, $onehot0, $isunknown), Constructs (ended, and, intersect, or, first_match, throughout, within, disableiff, expect, matched, if –else), assertion directives, nested implication, formal arguments in property.

SVA using local variables, calling subroutines, SVA for functional coverage, Connecting SVA to the Design or Test bench, SVA for FSMs, Memories, Protocol checkers, SVA Simulation Methodology, Assertions: Practice and Methodology, Re-use of Assertions, Tracking coverage with Assertions, Using SVA with other languages.

Functional Verification coverage using design, verification languages and implementation standards: Verilog IEEE 1364, VHDL IEEE 1076, System Verilog IEEE 1800, Property Specific Language (PSL) IEEE 1850, System C™ IEEE 1666, Encryption IEEE 1735, *e* Verification Language IEEE 1647, Open Verification Methodology (OVM) and Universal Verification Methodology (UVM).

Text Books

1. *Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for design: a guide to using System Verilog for hardware design and modelling", Springer, 2004.*
2. *Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", Springer, 2008.*
3. *Srikanth Vijayaraghavan and Meyyappan Ramanathan, "A Practical guide for System Verilog Assertions", Springer, 2005.*

Reference Books

1. *Janick Bergeron, "Writing test benches using System Verilog", Birkhäuser, 2006.*
2. *Ben Cohen, cohen, Venkataramanan, Kumari, Srinivasan Venkataramanan, Ajeetha Kumari, "SystemVerilog Assertions Handbook: for Formal and Dynamic Verification", vhdl cohen publishing, 2005.*
3. *Recent literature in Functional Verification using Hardware Verification Languages.*

Course outcomes

At the end of the course student will be able to

CO1: To learn about the testing environment of digital systems
CO2: To create test benches for digital systems
CO3: To learn about verification methodologies
CO4: To understand the need for system verification
CO5: To acquire digital verification skills

Course Code	**:**	**EC676**
Course Title	**:**	**Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To expose the students to all aspects of testing analog/mixed-signal circuits.

Course Content

Overview of Mixed-signal Testing. DC and Parametric Measurements. DAC Testing: Basics of converter testing, Basic DC tests, Transfer curve tests, Dynamic DAC tests, DAC Architectures.

ADC Testing: ADC testing versus DAC testing, DC tests and Transfer curve tests, Dynamic ADC tests, ADC Architectures. Sampling Theory. DSP based testing: Advantages of DSP based testing, DSP, Discrete-time transforms, The Inverse FFT.

Analog Channel Testing. Fundamentals of RF Testing. Design for Test: Overview, Advantages of DFT, Digital Scan, Digital BIST, Digital DFT for Mixed-signal circuits, Mixed-signal boundary scan and BIST, Ad-hoc Mixed signal DFT, RF DFT.

High speed design techniques: High Speed Op-amps, High Speed op-amp applications, RF/IF Subsystems.

High Speed sampling and High Speed ADCs, High Speed DACs and DDS systems.

Text Books

1. *An Introduction to Mixed-signal IC test and Measurement - Mark Burns, Gordon W. Roberts*
2. *High Speed Design Techniques - Walt Kester, Analog Devices*

Reference Books

1. *Linda S. Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing", IEEE Transactions on circuits and systems-II: Analog and Digital signal processing, Vol. 45, No. 10, October 1998.*
2. *The Fundamentals of Mixed Signal Testing - Brian Lowe*
3. *Test and Design for Testability in Mixed Signal ICs - Jose L Huertas*
4. *High Speed* Analog Design and Application Seminar - Texas Instruments.
5. *Recent literature in Testability of Analog / Mixed-Signal Circuits and High Speed Circuit Design.*

Course outcomes

At the end of the course student will be able to
CO1: To understand the testing methodology
CO2: To build test systems
CO3: To understand the requirements for BIST
CO4: To learn about error correction mechanisms
CO5: To understand the benefits of BIST

Course Code	**:**	**EC677**
Course Title	**:**	**High Speed System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To expose the students to all aspects of electronic packaging including electrical, thermal, mechanical and reliability issues.

Course Content

Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates

Overview of Transmission line theory, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI; crosstalk and nonideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise.

Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Design Process Electrical Design: Interconnect Capacitance, Resistance and Inductance fundamentals; Transmission Lines, Clock Distribution, Noise Sources, power Distribution, signal distribution, EMI, Digital and RF Issues. Processing Technologies, Thin Film deposition, Patterning, Metal to Metal joining.

IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging, reliability, wafer level burn – in and test. Single chip packaging: functions, types, materials processes, properties, characteristics, trends. Multi chip packaging: types, design, comparison, trends. Passives: discrete, integrated, embedded –encapsulation and sealing: fundamentals, requirements, materials, processes

Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation – Cooling requirements.

Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue – failures – thermo mechanically induced – electrically induced – chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

Text Book

1. *Tummala, Rao R., "Fundamentals of Microsystems Packaging", McGraw Hill, 2001*
2. *Howard Johnson, Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993*

Reference Books

1. *Blackwell (Ed), "The electronic packaging handbook", CRC Press, 2000.*
2. *Tummala, Rao R, "Microelectronics packaging handbook", McGraw Hill, 2008.*
3. *Bosshart, "Printed Circuit Boards Design and Technology", Tata McGraw Hill, 1988.*
4. *R.G. Kaduskar and V.B.Baru, "Electronic Product design", Wiley India, 2011*
5. *R.S.Khandpur, "Printed Circuit Board", Tata McGraw Hill, 2005*
6. *Recent literature in Electronic Packaging.*

Course outcomes

At the end of the course student will be able to

CO1: design of PCBs which minimize the EMI and operate at higher frequency.

CO2: design of packages which can withstand higher temperature, vibrations and shock.

CO3: explain the basic techniques for statistical process control and failure mode and effect analysis.

CO4: prescribe and perform parametric test and analysis and the troubleshooting of electronic circuits with the application of basic and virtual electronic instruments

CO5: explain contemporary pragmatic manufacturing processes, interconnects and assembly methods for electronic equipment fabrication.

Course Code	**:**	**EC678**
Course Title	**:**	**Modelling of Solid-State Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Objectives

- To study and model MOS Transistors and MOS Capacitors
- To understand the various CMOS design parameters and their impact on performance of the device.
- To study the device level characteristics of BJT transistors

Course Content

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non-equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunnelling, Tunnelling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields.

MOSFET Scaling, Constant-Field Scaling, Generalized Scaling, Non-scaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Non-uniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements

Basic CMOS Circuit Elements, CMOS Inverters, CMOS NAND and NOR Gates, Inverter and NAND Layouts, Parasitic Elements, Source–Drain Resistance, Parasitic Capacitances, Gate Resistance, Interconnect R and C, Sensitivity of CMOS Delay to Device Parameters, Propagation Delay and Delay Equation, Delay Sensitivity to Channel Width, Length, and Gate Oxide Thickness, Sensitivity of Delay to Power-Supply Voltage and Threshold Voltage, Sensitivity of Delay to Parasitic Resistance and Capacitance, Delay of Two-Way NAND and Body Effect, Performance Factors of Advanced CMOS Devices, MOSFETs in RF Circuits, Effect of Transport Parameters on CMOS Performance, Low-Temperature CMOS

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non-ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor, Relation Between B_{VCEO} and B_{VCBO}.

Reference Books:

1. Behzad Razavi, "Fundamentals of Microelectronics", Wiley Student Edition, 2nd Edition, 2008.
2. J P Collinge, C A Collinge, "Physics of Semiconductor devices" Springer 2002 Edition.
3. Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, Second Edition, 2009.

Course outcomes

At the end of the course student will be able to
CO1: To design and model MOSFET and BJT devices to desired specifications.
CO2: To understand the physics behind the device operation
CO3: To analyse the impact of the device physics in circuit design
CO4: To model novel semiconductor devices
CO5: To analyse the working of deep submicron semiconductor devices.

Course Code	**:**	**EC679**
Course Title	**:**	**Nano-Scale Devices: Modelling and Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Objectives

- To introduce novel MOSFET devices and understand the advantages of multi-gate devices
- To introduce the concepts of nanoscale MOS transistor and their performance characteristics
- To study the various nano-scaled MOS transistor circuits

Course Content

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

Silicon nanowire MOSFETs – Evaluation of I-V characteristics – The I-V characteristics for non-degenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors

Radiation effects in SOI MOSFETs, total ionizing dose effects – single-gate SOI – multi-gate devices, single event effect, scaling effects

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

Reference Books:

1. J P Colinge, "FINFETs and other multi-gate transistors", Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom, Jing Guo, "Nanoscale Transistors: Device Physics, Modelling and Simulation", Springer, 2006
3. M S Lundstorm, "Fundamentals of Carrier Transport", 2nd Ed., Cambridge University Press, Cambridge UK, 2000

Course Outcomes

At the end of the course student will be able to
CO1: study the MOS devices used below 10nm and beyond with an eye on the future
CO2: understand and study the physics behind the operation of multi-gate systems.
CO3: design circuits using nano-scaled MOS transistors with the physical insight of their functional characteristics
CO4: To appreciate the growth of scaling in MOSFETs
CO5: To understand the physical effects in deep sub-micron MOS devices

Course Code	**:**	**EC680**
Course Title	**:**	**Embedded System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Objective

- Ability to understand the technologies and techniques underlying in developing an embedded system.

Course Content

Introduction to Embedded system, embedded system examples, Parts of Embedded System Typical Processor architecture, Power supply, clock, Cache memory, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC etc. Bus architecture -I^2C, SPI, AMBA, CAN. Memory Technologies – EPROM, Flash, OTP, SRAM, DRAM, SDRAM etc.

Introduction to Cypress Programmable System on Chip (PSoC). Structure of PSoC, PSoC Designer, PSoC Modules, Interconnects, Memory Management, Global Resources, Design Examples
Embedded System product Development Life cycle (EDLC), Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure Design and Development. Concept of firmware, operating system and application programs. Power supply Design. External Interfaces.
Basic Features of an Operating System, Kernel Features [polled loop system, interrupt driven system, multi rate system], Processes and Threads, Context Switching, Scheduling [RMA, EDF, fault tolerant scheduling], Inter-process Communication, real Time memory management [process stack management, dynamic allocation], I/O [synchronous and asynchronous I/O, Interrupts Handling,Device drivers], RTOS [VxWorks, RT-LINUX].

Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT) etc.

Text Books

1. Shibu, "K.V. Introduction to Embedded Systems", Tata McGraw Hill, 2009
2. Marilyn Wolf, "Computers as components: Principles of Embedded Computing System Design" Elsevier, 2012.
3. Raj Kamal, "Embedded systems Architecture, Programming and Design", 2nd Edition, 2008
4. Lyla B Das, "Embedded Systems: An Integrated Approach", Pearson, 2013
5. Robert Ashby, "Designer's Guide to the Cypress PSoC Newnes", An imprint of Elsevier, 2006.
6. Oliver H. Bailey, "The Beginner's Guide to PSoC Express" Timelines Industries Inc., 1st Edition, 2007.

Course outcomes

At the end of the course student will be able to
CO1: define an embedded system and compare with general purpose system.
CO2: appreciate the methods adapted for the development of a typical embedded system.
CO3: get introduced to RTOS and related mechanisms.
CO4: To build embedded systems for real-time applications
CO5: To debug digital embedded systems and solve complex problems.

Course Code	**:**	**EC681**
Course Title	**:**	**Internet of Things**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Objective

- To give an exposure on the infrastructure, sensor technologies and networking technologies of IoT.
- To analyse, design and develop IOT solutions.
- To apply the concept of Internet of Things in the real world scenarios.

Course Content

Definition and Characteristics of IoT - Challenges and Issues - Physical Design of IoT, Logical Design of IoT - IoT Functional Blocks, Security.

Control Units – Communication modules – Bluetooth – Zigbee – Wifi – GPS- IOT Protocols (IPv6, 6LoWPAN, RPL, CoAP etc.), MQTT, Wired Communication, Power Sources.

Four pillars of IOT paradigm, - RFID, Wireless Sensor Networks, SCADA (Supervisory Control and Data Acquisition), M2M - IOT Enabling Technologies - BigData Analytics, Cloud Computing, Embedded Systems.

Working principles of sensors – IOT deployment for Raspberry Pi /Arduino/Equivalent platform – Reading from Sensors, Communication: Connecting microcontroller with mobile devices – communication through Bluetooth, wifi and USB - Contiki OSCooja Simulator.

Clustering, Clustering for Scalability, Clustering Protocols for IOT.

The Future Web of Things – Set up cloud environment –Cloud access from sensors– Data Analytics for IOT- Case studies- Open Source ‘e-Health sensor platform’ – ‘Be Close Elderly monitoring’ – Other recent projects.

Text Books

1. *Dieter Uckelmann et.al, “Architecting the Internet of Things”, Springer, 2011*
2. *Arshdeep Bahga and Vijay Madisetti, “Internet of Things – A Hand-on Approach”, Universities press, 2015.*

Reference Book

1. *Charalampos Doukas , “Building Internet of Things with the Arduino", Create space, April 2002*
2. *Dr. Ovidiu Vermesan and Dr. Peter Friess, “Internet of Things: From research and innovation to market deployment”, River Publishers 2014.*
3. *Contiki: The open source for IOT, www.contiki-os.org*

Course outcomes

At the end of the course student will be able to
CO1: identify the components of Internet of Things
CO2: development of IoT based application.
CO3: Build IoT based platforms for various use cases
CO4: Study the data gathered by IoT devices
CO5: Predict and dynamically optimize systems based on IoT data

Course Code	**:**	**EC682**
Course Title	**:**	**Semiconductor Memories**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Contents:

Memory hierarchy in digital systems; Static RAM: Types, Overall architecture, SRAM Cell - Design, Layout, Noise Issues and Margins and Assembly of Core, Peripheral Circuitry - Decoding, Array conditioning for read/write, Sensing, Writing, Synchronization;

Dynamic RAM: Types, Cell design, Assembly of core, Core architectures, Peripheral circuitry - Sensing, Elevated voltage supplies; Modern high speed DRAM - EDO, SDR, DDR;

Non Volatile Memories: ROM - Array Design, EPROM - Cell and Array Design, EEPROM -Tunnelling Phenomena, EEPROM Cell both Hot Carrier based operation and Tunnelling based Operation;

Flash Memories: Cell operation and design, Types of modern high density flash memories - NOR Flash, NAND Flash.

Reference Books:

1. *Betty Prince, "Semiconductor Memories: A Handbook of Design, Manufacture and Application", 2nd Edition, John Wiley,1996.*
2. *Betty Prince, "High Performance Memories: New Architecture DRAMs and SRAMs – Evolution and Function", Johm Wiley, 1999*
3. *Kiyoo Itoh, Masashi Horiguchi and Hitoshi Tanak, "Ultra-Low Voltage Nano-Scale Memories"' Springer International Edition, 2007*

Course outcomes

At the end of the course student will be able to
CO1: identify the parts of Memories
CO2: development of Semiconductor Memory architectures.
CO3: To learn the fundamental problems in memory design
CO4: develop novel circuit techniques for improving memory design
CO5: To understand and appreciate the growing semiconductor market for memory

Course Code	**:**	**EC683**
Course Title	**:**	**FPGA Based System Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To enable the students to understand the design and performance measures of FPGA based system design

Course Content

Overview of FPGA architectures and technologies: FPGA Architectural options, granularity of function and wiring resources, coarse vs fine grained, vendor specific issues (emphasis on Xilinx and Altera).

Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Power dissipation.

Programmable interconnect - Partitioning and Placement, Routing resources, delays; Applications - Embedded system design using FPGAs, DSP using FPGAs. Dynamic architecture using FPGAs, reconfigurable systems, application case studies. Simulation / implementation exercises of combinational, sequential and DSP kernels on Xilinx / Altera boards.

Hybrid architectures: Hybrid architectures, Communication, HW/SW partitioning, Soft-core microprocessors.

System architectures: System design strategies, Small-scale architectures, HPC architectures, Architectural design space explorations.
Special Topics: Numerical Analysis, Performance Analysis/Prediction, Fault Tolerance.

Text Book

1. *David Harris and Sarah Harris, “"Digital Design and Computer Architecture" Morgan Kaufmann; 2nd edition, 24 August 2012.*
2. *Wayne Wolf, “FPGA-Based System Design" Prentice Hall; Har/Cdr edition, 2004.*
3. *Pong P. Chu, “FPGA Prototyping by VHDL Examples" JOHN WILEY & SONS, INC., PUBLICATION, 2008.*

Reference Books

4. *Peter Athanas, Dionisios Pnevmatikatos, Nicolas Sklavos, “Embedded Systems Design with FPGAs”, Springer, 2012.*
5. *Ammar Mohammed and Abbes Amira "FPGA Architecture: Survey and Challenges," 2020.*

Course outcomes

At the end of the course student will be able to
CO1: acquire the basics of Multi rate Digital Signal Processing.
CO2: understand the concepts of Filter Banks and its applications.
CO3: understand the concepts and algorithms of Adaptive Filter theory.
CO4: understand the basics of Digital waveform synthesis and appreciate its applicability to various communication systems.
CO5: understand the concepts of Digital Down converters and Demodulators.

Course Code	**:**	**EC684**
Course Title	**:**	**Bio-Medical CMOS ICs**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To develop skills to design biomedical IC circuits

Course Content

Introduction to Bio-Medical CMOS Ics: Introduction to Bioelectricity, Electrical Properties of the Human body, Equivalent Circuit Model of Tissues and Organs, Biomedical Devices, Current Research Trends in Biomedical Electrical Instruments.

Electrode Design, Modern Disposable Electrodes, Solid Conductive Adhesive Electrodes, Implant Electrodes, Microelectrodes, Electrode Standards.

Readout circuits: Biopotential Acquisition, Power Efficient Instrumentation Amplifier Topologies for Biopotential Signal Extraction, Current Mode Instrumentation Amplifiers,
Examples of ICs for Biopotential Acquisition.

Basic operation principles and architectures as well as the most recent research results of low power CMOS ICs. Low power ADCs for Bio-Medical Applications, Low Power Bio-Medical DSP.

Bio-Medical Wireless Communication, Introduction to Short distance Wireless Communications.

Text Books

1. *Hoi-Jun Yoo: Chris van Hoof, "Integrated Circuits and Systems- Bio Medical CMOS ICs", Springer, 2010*
2. *D C Reddy "Biomedical Signal Processing: Principles and Techniques", Tata McGraw-Hill Publishing Co. Ltd, 2005*

Reference Books

1. *R M Rangayyan, "Biomedical Signal Analysis: A case Based Approach", IEEE Press, John Wiley and Sons. Inc., 2002*
2. *Jacob Fraden, "Handbook of Modern Sensors: Physics, Designs, and Applications", Springer, 2010*
3. *J. G. Webster, "The Measurement, Instrumentation and Sensors Handbook vol. 1", CRC Press, 1st Edition, 1998*

Course outcomes

At the end of the course student will be able to

CO1: familiarise the concepts of used to design biomedical ICs
CO2: acquire knowledge to design various electrodes
CO3: learn the design of various biomedical amplifiers
CO4: analyse and implement various low power ADCs for biomedical applications
CO5: acquire knowledge about types of short range wireless communication

Course Code	**:**	**EC685**
Course Title	**:**	**On-chip Antenna Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To make the students understand the basic concepts and design procedures of on-chip antennas.
- Introduce the students to various packaging technologies for on-chip antennas

Course Content

Introduction to millimetre wave technologies: Antenna, RF Electronics, Packaging, Millimetre wave packaging, Review of Microwave Packaging Technologies, Low-cost mm Wave Packaging, Emerging Packaging Technologies, Package Co-design at mm Waves.

Millimetre-wave Interconnects: Interconnects at Millimetre-wave Frequencies, Interconnect Technology Options for Millimetre-wave Applications, Performance-oriented Interconnect Technology Optimization, Chip-to-package Interconnects at Millimetre-wave Frequencies.

Printed Millimetre Antennas: Introduction and Considerations for Millimetre-wave Printed Antennas, Multilayer Interconnection Technology, Multilayer Antenna Array with Shaped Beam, Connector and Diffraction Problems for Printed Antennas.

Planar Waveguide-type Slot Arrays: Equivalent Length of a Round-ended Straight Slot, Alternating-phase Fed Single-layer Slotted Waveguide Array and its Side lobe Suppression, Centre Feed Single Layer Slotted Waveguide Array, Single-layer Hollow-waveguide Eight-way Butler Matrix, Radial Line Slot Antennas, Post-wall Waveguide-fed Parallel Plate Slot Arrays, Coaxial-line to Post-wall Waveguide Transformers.

Antenna Design for Packaging Applications: Air-suspended Superstrate Antenna, Packaged Antennas, A Patch Array, Circularly Polarized Antenna, Assembly Process, Advanced Packaging Application. Monolithic Integrated Antennas: Monolithic Antenna Integration Challenges, Manufacturing Techniques for Enhanced Antenna Performance, Circuit Integration, Packaging of Integrated Circuits with On-chip Antennas, Monolithic Antenna Measurement Techniques.
Phased Array: Antenna Element Design for Phased Arrays, Beam-forming Network, Design and Manufacture Issues Integrated Phased Arrays: Integrated Phased Arrays, Fully Integrated mm Wave Phased-array Transceiver, Direct Antenna Modulation, Large-scale Integrated Phased Arrays. CMOS RF Circuits- Integrated Transmitter and Receiver, Wireless Inter chip Interconnects.

Text Books

1. *Duixian Liu, Brian Gaucher, "Advanced millimetre wave technologies: Antennas, Packaging and Circuits", Wiley, 2012.*
2. *Mikhail R. Baklanov, Paul S. Ho, EhrenfriedZschech, "Advanced interconnects for ULSI Technology", Wiley, 2012.*

Reference Books

1) *Samee Ullah Khan, Joanna Kołodziej, Juan Li, Albert Y. Zomaya, "Evolutionary based solutions for green computing", Springer 2013.*

Course outcomes

At the end of the course student will be able to

CO1: Familiarise the effects of substrates on millimetre wave antennas
CO2: Design of interconnects at millimetre wave frequencies
CO3: Design millimetre wave printed antennas antennas
CO4: Enable design of antennas with packages
CO5: Acquire knowledge about antenna arrays and phased arrays

Course Code	**:**	**EC612**
Course Title	**:**	**DSP Architecture**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To give an exposure to the various fixed point and floating point DSP architectures and to implement real time applications using these processors.

Course Content

Fixed-point DSP architectures. TMS320C54X, ADSP21XX, DSP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses. TMS320C55X architecture and its comparison.

Floating-point DSP architectures. TMS320C67X, DSP96XX architectures. Cache architecture. Floating-point Data formats. On-chip peripherals. Memory Map and Buses.

On-chip peripherals and interfacing. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF. Serial interface- Audio codec. Sensors. A/D and D/A interfaces. Parallel interface- RAM and FPGA. RF transceiver interface.

DSP tools and applications. Implementation of Filters, DFT, QPSK Modem, Speech processing. Video processing, Video Encoding / Decoding. Biometrics. Machine Vision. High performance computing (HPC).

Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP. CORTEX, SHARC, SIMD, MIMD Architectures.

Text Books

1. *B.Venkataramani and M.Bhaskar, "Digital Signal Processor, Architecture, Programming and Applications", 2nd Edition, McGraw- Hill, 2010*
2. *S.Srinivasan and Avtar Singh, "Digital Signal Processing, Implementations using DSP Microprocessors with Examples from TMS320C54X", Brooks/Cole, 2004*

Reference Books

1. *S.M.Kuo and Woon-Seng S.Gan, "Digital Signal Processors: Architectures, Implementations, and Applications", Prentice Hall, 2004.*
2. *N. Kehtarnavaz and M. Kerama, "DSP System Design using the TMS320C6000", Prentice Hall, 2001.*
3. *S.M. Kuo and B. H.Lee, "Real-Time Digital Signal Processing, Implementations, Applications and Experiments with the TMS320C55X", John Wiley, 2001.*
4. *Recent literature in DSP Architecture.*

Course outcomes

At the end of the course student will be able to

CO1: learn the architecture details fixed and floating point DSPs

CO2: infer about the control instructions, interrupts, and pipeline operations, memory and buses.

CO3: illustrate the features of on-chip peripheral devices and its interfacing with real time application devices.

CO4: learn to implement the signal processing algorithms and applications in DSPs.

CO5: learn the architecture of advanced DSPs.

Course Code	**:**	**EC613**
Course Title	**:**	**High Speed Communication Networks**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To impart the students a thorough exposure to the various high speed networking technologies and to analyze the methods adopted for performance modeling , traffic management and routing

Course Content

The need for a protocol architecture, The TCP/IP protocol architecture, Internetworking,
Packet switching networks, Frame relay networks, Asynchronous Transfer mode (ATM) protocol architecture, High speed LANs. Multistage networks

Overview of probability and stochastic process, Queuing analysis, single server and multi-server queues, queues with priorities, networks of queues, Self similar Data traffic

Congestion control in data networks and internets, Link level flow and error control, TCP traffic control, Traffic and congestion control in ATM networks

Overview of Graph theory and least cost paths, Interior routing protocols, Exterior routing protocols and multicast.

Quality of service in IP networks, Integrated and differentiated services, Protocols for QOS support-Resource reservation protocol, Multiprotocol label switching, Real time transport protocol.

Text Books

1. *W. Stallings, "High Speed networks and Internets", second edition, Pearson Education, 2002.*
2. *A. Pattavina, "Switching Theory", Wiley, 1998.*
3. *J. F. Kurose and K. W. Ross, "Computer networking", 3rd Edition, Pearson education,2005*

Reference Books

1. *Mischa Schwartz, "Telecommunication networks, protocols, modeling and analysis", Pearson education,2004*
2. *Giroux, N. and Ganti, S, "Quality of service in ATM networks", Prentice Hall ,1999*
3. *Recent literature in High Speed Communication Networks.*

Course outcomes

At the end of the course student will be able to

CO1: compare and analyze the fundamental principles of various high speed communication networks and their protocol architectures
CO 2: analyze the methods adopted for performance modeling of traffic flow and estimation
CO 3: examine the congestion control issues and traffic management in TCP/IP and ATM networks
CO 4: compare, analyze and implement the various routing protocols in simulation software tools
CO 5: examine the various services.

Course Code	**:**	**EC615**
Course Title	**:**	**Digital Image Processing**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To explore various techniques involved in Digital Image Processing.

Course Content

Elements of Visual perception. Image sensing and Acquisition. Imaging in different bands. Digital Image Representation. Relationship between pixels. Image transformations: 2D-DFT, DCT, DST, Hadamard, Walsh, Hotelling transformation, 2D-Wavelet transformation, Wavelet packets.

Image Enhancements in spatial domain and Frequency domain. Image Restoration techniques. Color Image processing.

Error free compression: Variable length coding, LZW, Bit-plane coding, Lossless predictive coding Lossy compression: Lossy predictive coding, transform coding, wavelet coding. Image compression standards (CCITT, JPEG, JPEG 2000) and Video compression standards.

Summary of morphological operations in Binary and Gray Images. Image segmentation: Point, Line and Edge segmentation. Edge linking and Boundary detection. Segmentation using thresholding, Region based segmentation. Segmentation by morphological watersheds. Use of motion in segmentation.

Feature Extraction from the Image: Boundary descriptors, Regional descriptors, Relational descriptors. Dimensionality reduction techniques, Discriminative approach and the Probabilistic approach for image pattern recognition.

Text Books

1. *R. C.Gonzalez, R.E.Woods," Digital Image processing", Pearson edition, Inc3/e, 2008.*
2. *A.K.Jain," Fundamentals of Digital Image Processing", PHI,1995*

Reference Books

1. *J.C. Russ, "The Image Processing Handbook", 5th Edition, CRC, 2006*
2. *R.C.Gonzalez and R.E. Woods; "Digital Image Processing with MATLAB", Prentice Hall, 2003*
3. *E.S.Gopi, "Digital Image processing using Matlab", Scitech publications, 2005*
4. *Recent literature in Digital Image Processing.*

Course outcomes

At the end of the course student will be able to

CO1: understand the need for image transforms different types of image transforms and their properties.
CO2: develop any image processing application.
CO3: understand the rapid advances in Machine vision.
CO4: learn different techniques employed for the enhancement of images.
CO5: learn different causes for image degradation and overview of image restoration techniques.

Course Code	**:**	**EC616**
Course Title	**:**	**RF MEMS**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To impart knowledge on basics of MEMS and their applications in RF circuit design.

Course Content

Micromachining Processes - methods, RF MEMS relays and switches. Switch parameters. Actuation mechanisms. Bistable relays and micro actuators. Dynamics of switching operation.

MEMS inductors and capacitors. Micro-machined inductor. Effect of inductor layout. Modelling and design issues of planar inductor. Gap-tuning and area-tuning capacitors. Dielectric tunable capacitors.

MEMS phase shifters. Types. Limitations. Switched delay lines. Fundamentals of RF MEMS Filters.

Micro-machined transmission lines. Coplanar lines. Micro-machined directional coupler and mixer.

Micro-machined antennas. Microstrip antennas – design parameters. Micromachining to improve performance. Reconfigurable antennas.

Text Book

1. *Vijay. K. Varadan, K.J. Vinoy, and K.A. Jose, "RF MEMS and their Applications", Wiley-India, 2011.*

Reference Books

1. *H. J. D. Santos, "RF MEMS Circuit Design for Wireless Communications", Artech House, 2002.*
2. *G. M. Rebeiz, "RF MEMS Theory, Design, and Technology", Wiley, 2003.*
3. *Recent literature in RF MEMS.*

Course outcomes

At the end of the course student will be able to
CO1: learn the Micromachining Processes
CO2: learn the design and applications of RF MEMS inductors and capacitors.
CO3: learn about RF MEMS Filters and RF MEMS Phase Shifters.
CO4: learn about the suitability of micro-machined transmission lines for RF MEMS
CO5: learn about the Micro-machined Antennas and Reconfigurable Antennas.

Course Code	**:**	**EC626**
Course Title	**:**	**Bio MEMS**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective

- To train the students in the design aspects of Bio MEMS devices and Systems. To make the students aware of applications in various medical specialists especially the Comparison of conventions methods and Bio MEMS usage.

Course Content

Introduction-The driving force behind Biomedical Applications – Biocompatibility - Reliability Considerations-Regularity Considerations – Organizations - Education of Bio MEMS-Silicon Micro fabrication-Soft Fabrication techniques

Micro fluidic Principles- Introduction-Transport Processes- Electro kinetic Phenomena-Micro valves – Micro mixers- Micro pumps.

SENSOR PRINCIPLES and MICRO SENSORS: Introduction-Fabrication-Basic Sensors-Optical fibers-Piezo electricity and SAW devices-Electrochemical detection-Applications in Medicine

MICRO ACTUATORS and DRUG DELIVERY: Introduction-Activation Methods-Micro actuators for Micro fluidics-equivalent circuit representation-Drug Delivery

MICRO TOTAL ANALYSIS: Lab on Chip-Capillary Electrophoresis Arrays-cell, molecule and Particle Handling-Surface Modification-Microsphere-Cell based Bioassay Systems
Detection and Measurement Methods-Emerging Bio MEMS Technology-Packaging, Power, Data and RF Safety-Biocompatibility, Standards

Text Book

1. *Steven S. Saliterman, "Fundamentals of Bio MEMS and Medical Micro devices", Wiley Inter science, 2006.*

Reference Books

1. *Albert Folch , "Introduction to Bio MEMS", CRC Press, 2012*
2. *Gerald A. Urban, "Bio MEMS", Springer, 2006*
3. *Wanjun wang, steven A. Soper, "Bio MEMS", 1st Edition, CRC Press, 2006.*
4. *M. J. Madou, "Fundamental of Micro fabrication", 2nd Edition, CRC Press, 2002.*
5. *G.T. A. Kovacs, "Micro machined Transducers Sourcebook", 1st Edition, McGraw Hill, 1998.*
6. *Recent literature in Bio MEMS.*

Course outcomes

At the end of the course student will be able to
CO1: learn and realize the MEMS applications in Bio Medical Engineering
CO2: understand the Micro fluidic Principles and study its applications.
CO3: learn the applications of Sensors in Health Engineering.
CO4: learn the principles of Micro Actuators and Drug Delivery system
CO5: learn the principles and applications of Micro Total Analysis

Course Code	**:**	**EC628**
Course Title	**:**	**Pattern Recognition and Computational Intelligence**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE OBJECTIVE

- The subject aims to make the students to understand the mathematical approach for pattern recognition. and computational intelligence

COURSE CONTENT

Polynomial curve fitting – The curse of dimensionality - Decision theory - Information theory - The beta distribution - Dirichlet distribution-Gaussian distribution-The exponent family: Maximum likelihood and sufficient statistics -Non-parametric method: kernel-density estimators - Nearest neighbour methods.

Linear models for regression and classification: Linear basis function models for regression - Bias variance decomposition-Bayesian linear regression-Discriminant functions - Fisher's linear discriminant analysis (LDA) - Principal Component Analysis (PCA) - Probabilistic generative model - Probabilistic discriminative model- Independent Component Analysis (ICA)

Kernel methods: Dual representations-Constructing kernels-Radial basis function networks-Gaussian process-Maximum margin classifier (Support Vector Machine) –Relevance Vector Machines-Kernel-PCA, Kernel-LDA.

Mixture models: K-means clustering - Mixtures of Gaussian - Expectation-Maximization algorithm-Sequential models: Markov model, Hidden-Markov Model (HMM) - Linear Dynamical Systems (LDS).

Neural networks: Feed- forward Network functions-Network training - Error Back propagation - The Hessian Matrix - Regularization in Neural Network - Mixture density networks – Bayesian Neural Networks - Particle swarm optimization-Genetic algorithm-Ant colony optimization-Bacterial foroging-Simulated annealing – Fuzzy logic systems

Text Books

1. *C.M.Bishop, "Pattern recognition and machine learning", Springer, 2006*
2. *E.S.Gopi, "Pattern recognition and Computational intelligence using matlab, Transactions on computational science and computational intelligence, Springer, 2019*

Reference Books

1. *Sergious Thedorodis, Konstantinos Koutroumbas, Pattern recognition, Elsevier, Fourth edition, 2009*
2. *Richard O.Duda, Peter.E.Hart, David G.Stork, "Pattern classification", Wiley, Second edition, 2016*
3. *E.S.Gopi, "Algorithm collections for Digital signal Processing application using Matlab"- Springer, 2007*
4. *Recent literature in the related topics*

COURSE OUTCOMES

Students are able to

CO1: summarize the various techniques involved in pattern recognition

CO2: identify the suitable pattern recognition techniques for the particular applications.

CO3: categorize the various pattern recognition techniques into supervised and unsupervised.

CO4: summarize the mixture models based pattern recognition techniques

CO5: summarize the various computational intelligence techniques for pattern recognition

Course Code	**:**	**EC632**
Course Title	**:**	**Foundations of Artificial Intelligence**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE OBJECTIVE

- Approaches to produce "intelligent" systems, Knowledge representation (both symbolic and neural network), search and machine learning.
- To learn the principles and fundamentals of designing AI programs.

COURSE CONTENT

Introduction to artificial Intelligence, problem solving as state space search, Uninformed search, heuristic search, informed search, constrained satisfaction problem

Knowledge representation and Reasoning-Introduction to knowledge representation, propositional logic, first order logic, inference in first order logic, answer extraction, procedural control of reasoning, reasoning under uncertainty, Bayesian network, decision network.

Planning and decision making- Introduction to planning, plan space planning, planning graph and graph plan, practical planning and acting, sequential decision problems, making complex decisions.

Machine learning- Introduction to ML, learning decision trees, linear regression, SVM, supervised learning, unsupervised learning, reinforcement learning,

Introduction to deep learning and neural network learning

Text Books

1. *Patrick Henry Winston, Artificial Intelligence, Third Edition, Addison-Wesley Publishing Company, 2004.*
2. *Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, 3rd Edition, PHI 2009.*

Reference Books

1. *Nils J Nilsson, Principles of Artificial Intelligence, Illustrated Reprint Edition, Springer Heidelberg, 2014.*
2. *Nils J. Nilsson, Quest for Artificial Intelligence, First Edition, Cambridge University Press, 2010.*

COURSE OUTCOMES

Students are able

CO1: To learn the concepts of artificial intelligence

CO2: To study problem solving techniques

CO3: To understand the representation of knowledge and reasoning mechanism

CO4: To learn to panning and decision making

CO5: To study network models used for learning

Course Code	**:**	**EC635**
Course Title	**:**	**Electromagnetic Interference and Compatibility**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE OBJECTIVE

- Electromagnetic interference (EMI) is a potential threat to the present day electronic systems. The main objective of the course is to provide insight into various sources of electromagnetic interferences and how to design an electronic product which is electromagnetically compatible with each other.

COURSE CONTENT

Introduction to EMI and EMC- Various EMC requirements and standards-Need for EMC and its importance in electronic product design - sources of EMI - few case studies on EMC.

Conducted and radiated emission -power supply line filters-common mode and differential mode current-common mode choke- switched mode power supplies. Shielding techniques- shielding effectiveness-shield behavior for electric and magnetic field -aperture-seams-conductive gaskets-conductive coatings
Grounding techniques- signal ground-single point and multi point grounding-system ground-common impedance coupling -common mode choke-Digital circuit power distribution and grounding.

Contact protection - arc and glow discharge-contact protection network for inductive loads-C, RC, RCD protection circuit- inductive kick back. RF and transient immunity-transient protection network- RFI mitigation filter-power line disturbance- ESD- human body model- ESD protection in system design.

PCB design for EMC compliance-PCB layout and stack up- multi layer PCB objectives- Return path discontinuities-mixed signal PCB layout. EMC pre compliance measurement-conducted and radiated emission test-LISN-Anechoic chamber.

Text Books:

1. *H. W. Ott, Electromagnetic Compatibility Engineering, 2nd edition, John Wiley & Sons, 2011, ISBN: 9781118210659.*
2. *C. R. Paul, Introduction to Electromagnetic Compatibility, 2nd edition, Wiley India, 2010, ISBN: 9788126528752*

Reference Book:

1. *K. L. Kaiser, Electromagnetic Compatibility Handbook, 1st edition, CRC Press, 2005. ISBN: 9780849320873*

COURSE OUTCOMES

Students are able to

CO1: Understand the various sources of Electromagnetic interference

CO2: Familiarize the fundamentals those are essential for product design with EMC compliance and various EMC standards

CO3:. would gain knowledge to understand the concept of Shielding and grounding related to product design.

CO4:. Design PCBs which are electromagnetically compatible

CO5: understand and differentiate the various EMC pre compliance measurement

Course Code	**:**	**EC636**
Course Title	**:**	**Computer Vision**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE OBJECTIVE

- The focus of this course is the understanding of algorithms and techniques used in computer vision.
- Provide pointers into the literature and exercise a project based on a literature search and one or more research papers.
- Practice software implementation of different concepts and techniques covered in the course.
- Utilize programming and scientific tools for relevant software implementation.

COURSE CONTENT

Introduction: overview of computer vision, related areas, and applications; overview of software tools; overview of course objectives.; introduction to OpenCV. Image formation and representation: imaging geometry, radiometry, digitization, cameras and projections, rigid and affine transformations, Filtering: convolution, smoothing, differencing, and scale space

Feature detection: edge detection, corner detection, line and curve detection, active contours, SIFT and HOG descriptors, shape context descriptors, Model fitting: Hough transform, line fitting, ellipse and conic sections fitting, algebraic and Euclidean distance measures.

Camera calibration: camera models; intrinsic and extrinsic parameters; radial lens distortion; direct parameter calibration; camera parameters from projection matrices; orthographic, weak perspective, affine, and perspective camera models.

Motion analysis: the motion field of rigid objects; motion parallax; optical flow, the image brightness constancy equation, affine flow; differential techniques; feature-based techniques; regularization and robust estimation; motion segmentation through EM, Motion tracking: statistical filtering; iterated estimation; observability and linear systems; the Kalman filter; the extended Kalman filter

Object recognition and shape representation: alignment, appearance-based methods, invariants, image Eigen spaces, data-based techniques.

Text Books

1. *Computer Vision: Algorithms and Applications, R. Szeliski, Springer, 2011.*
2. *Computer Vision: A Modern Approach, D. Forsyth and J. Ponce, Prentice Hall, 2nd ed., 2011.*
3. *Introductory techniques for 3D computer vision, E. Trucco and A. Verri, Prentice Hall, 1998.*

COURSE OUTCOMES

Students are able
CO1: To understand the fundamental problems of computer vision.
CO2: To learn techniques, mathematical concepts and algorithms used in computer vision to facilitate further study in this area.
CO3: To get an idea regarding the camera calibration and its importance.
CO4: To study different kinds of motion estimation methodologies and its applications.
CO5: To understand the basic concepts of object and shape recognition techniques

Course Code	**:**	**EC637**
Course Title	**:**	**Natural Language Processing**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE LEARNING OBJECTIVE

- Understand NLP tasks in syntax, semantics and pragmatics
- Implement machine learning techniques used in NLP

Introduction – Why NLP? NLP versus speech recognition- Applications-problem of ambiguity- role of machine learning in NLP- Basic neural networks for NLP

Words – Morphology and Finite State transducers-Tokenization – Computational Phonology and Pronunciation Modelling

Probabilistic models in NLP — Role of language models- Simple N-gram model – Evaluation: Perplexity and Word Error Rate. Parts of Speech Tagging- Hidden markov models–Viterbi algorithm, Maximum Entropy Markov model

Semantic analysis - Lexical semantics and word-sense disambiguation. Compositional semantics. Semantic Role Labeling and Semantic Parsing

Machine Translation - Statistical translation, word alignment, phrase-based translation, and synchronous grammars, evaluation.

Reference Books

1. Natural Language Processing, by Jacob Eisenstein, MIT Press.
2. Speech and Language Processing by Daniel Jurafsky and James H. Martin
3. Foundations of Statistical Natural Language processing by Manning C. D. and Schutze H., First Edition, MIT Press, 1999
4. Neural Network Methods for Natural Language Processing by Yoav Goldberg, Morgan & Claypool Publishers.

COURSE OUTCOMES

Students are able to
CO1: Understand NLP and the role of machine learning in NLP
CO2: Describe finite state transducer operations and pronunciation modelling in NLP
CO3: Illustrate various probabilistic models in NLP.
CO4: Study semantic analysis in NLP
CO5: Learn various machine translation approaches and the different evaluation metrics.

Course Code	**:**	**EC638**
Course Title	**:**	**Optimization Methods In Machine Learning**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE LEARNING OBJECTIVE

- The course aims to equip students with advanced techniques and methods in optimization that are tailored to large-scale statistics and machine learning problems

COURSE CONTENT

Basics of convex optimization- convex sets, convexity-preserving operations, examples of convex programs (linear programming (LP), second-order cone programming (SOCP), semidefinite programming (SDP)), convex relaxation, KKT conditions, duality

Gradient-based methods- gradient descent, subgradient, mirror descent, Frank–Wolfe method, Nesterov's accelerated gradient method, ODE interpretations, dual methods, Nesterov's smoothing, proximal gradient methods, Moreau–Yosida regularization

Operator splitting methods- augmented Lagrangian methods, alternating direction method of multipliers (ADMM), monotone operators, Douglas–Rachford splitting, primal and dual decomposition

Stochastic and nonconvex optimization-dual averaging, Polyak–Juditsky averaging, stochastic variance reduced gradient (SVRG), Langevin dynamics, escaping saddle points, landscape of nonconvex problems, deep learning

Applications of optimization methods in Image/Video/Multimedia Processing

Textbooks:

1. *Stephen Boyd and Lieven Vandenberghe's book: Convex Optimization*
2. *Nesterov's old book: Introductory Lectures on Convex Optimization: A Basic Course*
3. *Nesterov's new book: Lectures on Convex Optimization*
4. *Neal Parikh and Stephen Boyd's monograph: Proximal Algorithms*
5. *Sebastien Bubeck's monograph: Convex Optimization: Algorithms and Complexity*

References

1. *Moritz Hardt's Berkeley EE 227C course note*
2. *Prateek Jain and Purushottam Kar's survey on nonconvex optimization*
3. *Kristin Bennett, Emilio Parrado-Hernandez. Interplay of Optimization and Machine Learning Research, Journal of Machine Learning Research, 2006.*
4. *Nati Srebro, Ambuj Tewari. Stochastic Optimization for Machine Learning, Tutorial at International Conference on Machine Learning, 2010.*

COURSE OUTCOMES

Students are able

CO1: To learn the basic concepts of convex optimization

CO2: To study gradient based optimization techniques

CO3: To understand the problem solving using operator splitting methods

CO4: To learn stochastic and non-convex optimization Techniques,

CO5: To execute applications of optimization techniques in different domains

Course Code	**:**	**EC639**
Course Title	**:**	**Hardware for Deep Learning**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE LEARNING OBJECTIVE

To get an idea about deep learning and how to implement deep learning algorithms on FPGA

COURSE CONTENT

Introduction to Deep Learning: From AI to DL, Neural Network: Perceptrons, Back Propagation, Over-fitting, Regularization. Deep Networks: Definition, Motivation, Applications, Convolution Neural Network (CNN): Basic architecture, Activation functions, Pooling, Handling vanishing gradient problem, Dropout, Weight initialization methods, Batch Normalization. Training Neural networks, Additional CNN Components, Famous CNNs, Applications, Software libraries.

Computing Convolutions: Mapping Matrix multiplication, Computational Transforms, Accelerator Architectures, Dataflow Taxonomy

Reducing the Complexity: Light weight models, reducing precision, Aggressive Quantization, pruning & Deep compression.

The Deep Learning Acceleration Landscape: parallelism in deep learning, Traditional programmable hardware, specialized deep learning hardware platforms, deep learning software stack, Specialized research ASICs.

FPGAs for Deep Learning: Overview of hardware architectures for deep learning, Effective management of FPGA memory resources, optimizing algorithms and data representation for FPGA arithmetic resources, Integrating hardware and software.

Text Books

1. *Ian Goodfellow, Yishuv Bengio and Aaron Courville, "Deep Learning." MIT Press. 2016. ISBN: 978-0262035613. Available online for free at: http://www.deeplearningbook.org*
2. *Vivienne Sze; Yu-Hsin Chen; Tien-Ju Yang; Joel S. Emer, "Efficient Processing of Deep Neural Networks" Morgan & Claypool Publishers, 1st Edition, 2020.*
3. *Tushar Krishna, Hyoukjun Kwon, Angshuman Parashar, Michael Pellauer, and Ananda Samajdar, "Data Orchestration in Deep Learning Accelerators", Morgan & Claypool Publishers, 1st Edition, 2020.*

References

4. *Piotr Antonik, "Application of FPGA to Real-Time Machine Learning", Springer, 2018.*
5. *Stanford C231n, 2017*
6. *Sze, et al. https://eyeriss.mit.edu/ ISCA Tutorial 2019*
7. *Sze, et al. "Efficient Processing of Deep Neural Networks: A Tutorial and Survey", Proceedings of the IEEE, 2017*
8. *Prof. Adam Teman https://www.eng.biu.ac.il/temanad/hardware-for-deep-learning/*
9. *https://jameswhanlon.com/*

Course outcomes

CO1: Understand the context of convolutional neural networks and deep learning algorithms.

CO2: Know how to use convolution in deep learning techniques.

CO3: Understand the necessity and importance of light weight models with low complexity through specialized hardware architecture

CO4: Know how to optimize hardware performance in deep neural network applications.CO5: Discuss, suggest and evaluate specialised hardware architectures to implement deep learning algorithms in FPGA and utilise deep learning concepts in resource constrained reliablesystems.

Course Code	**:**	**EC640**
Course Title	**:**	**Image and Video Processing**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE LEARNING OBJECTIVE

- The course aims to equip students with basic image and video processing techniques.

COURSE CONTENTS

Image Formation and Representation: 3D to 2D projection, photometric image formation, trichromatic colour representation, video format (SD, HD, UHD, HDR), contrast enhancement (concept of histogram, nonlinear mapping, histogram equalization)

Review of 1D Fourier transform and convolution: Concept of spatial frequency. Continuous and Discrete Space 2D Fourier transform. 2D convolution and its interpretation in frequency domain. Implementation of 2D convolution. Separable filters. Frequency response. Linear filtering (2D convolution) for noise removal, image sharpening, and edge detection. Gaussian filters, DOG and LOG filters as image.

Geometric mapping and Feature detection: Geometric mapping (affine, homography), Feature based camera motion estimation (RANSAC). Image warping. Image registration. Panoramic view stitching, Feature detection (Harris corner, scale space, SIFT), feature descriptors (SIFT). Bag of Visual Word representation for image classification.

Motion estimation: optical flow equation, optical flow estimation (Lucas-Kanade method, KLT tracker); block matching, multi-resolution estimation. Deformable registration (medical applications), Moving object detection (background/foreground separation): Robust PCA (low rank + sparse decomposition). Global camera motion estimation from optical flows. Video stabilization. Video scene change detection.

Video Coding: block-based motion compensated prediction and interpolation, adaptive spatial prediction, block-based hybrid video coding, rate-distortion optimized mode selection, rate control, Group of pictures (GoP) structure, tradeoff between coding efficiency, delay, and complexity, depth from disparity, disparity estimation, view synthesis. Multiview video compression. Depth camera (Kinect). 360 video camera and view stitching.

Text Book/References:

1. *Richard Szeliski, Computer Vision: Algorithms and Applications. (Available online:"Link") (Cover most of the material, except sparsity-based image processing and image and video coding)*
2. *(Optional) Y. Wang, J. Ostermann, and Y.Q.Zhang, Video Processing and Communications. Prentice Hall, 2002. "Link" (Reference for image and video coding, motion estimation, and stereo)*
3. *(Optional) R. C. Gonzalez and R. E. Woods, Digital Image Processing, Prentice Hall, (3rd Edition) 2008. ISBN number 9780131687288. "Link" (Good reference for basic image processing, wavelet transforms and image coding).*

COURSE OUTCOMES

Students are able to

CO1: Understand the concept of image formation and representation

CO2: Know the need of transformation and convolution

CO3: Understand the necessity and importance of feature detection and geometric mapping

CO4: Know how to do motion estimation in video

CO5: To understand the basic ideas of video coding

Course Code	**:**	**EC641**
Course Title	**:**	**Automated Test Engineering for Electronics**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

COURSE CONTENT

Printed Circuit Boards (PCBs) – types of PCB – multilayer PCBs – Plated though Hole Technology (PTH) - Surface Mount Technology (SMT) – Ball Grid Array (BGA) Technology. Bare PCB electrical test concepts, Loaded PCB Visual inspection, Automated Optical inspection systems, X-Ray inspection systems- Measuring Passive components – 2 wire, 3 wire, 4 wire and 6 wire measurement concepts, Guarding techniques, Shorts location, Most common manufacturing defects, Automated Manufacturing defect analyzers, Nodal Impedance / analog signature analysis. Flying probe testers.

Concepts of PCB Trouble-shooting, Symptom recognition, Bracketing technique, Failure types and fault causes, Manual Trouble shooting, Use of DMM, Oscilloscope, Signal Generators, Logic Probes, Logic Pulsers, Logic Analyzers, Automated Test Techniques – CPU Emulation technique, ROM Emulation, In-Circuit Comparators, In- Circuit Emulators, Functional Testing of Digital ICs, Library models, Concepts of In-circuit Testing, - Back Driving technique – international defence standards - Auto Compensation, In-Circuit Test of Open collector / Emitter Devices, Tri-State, Bi-Directional Devices, Concepts of Digital Guarding, Analog and Mixed Signal ICs Test, advantages and limitations of in-circuit testing, AC – DC Parametric testing, –Advanced test techniques- Boundary Scan Test , Learn and compare technique – digital signatures, Bus Cycle Signature Test , Analog signatures.

ATE system components, Main Test Vector processor, Digital Subsystem, Pin Electronics, Programmable drive and threshold levels, RAM behind each pin, Controlling slew rate, Skew between channels, Data formats, Digital and analog simulation, Test Vector Generation, Fault simulation, Fault coverage, Test Languages, Verilog, VHDL, Automatic compare, Analog Sub system, Digital and analog matrix switch circuits, digital and analog highways, Integration of JTAG, Boundary Scan Test, BSDL, External Instrumentation, Functional and Timing tests. Concepts of Test Program (T.P) Generation. Commercially available off the shelf Test Equipment's (COTS)

Board Functional Test (BFT) techniques – Go-No-go Test – Diagnostic Test, Reliability Test, Thermal Shock Test, Full functional Edge to edge test, Cluster Test – Guided Probe Backtracking Technique – Simulators – Online and Offline Simulation - Fault Simulation– Comprehensiveness of Board program – Fault Dictionary– Analysis – BS and Non-BS device testing–- Sample board programming and testing – BS interconnect and simulating faults - External Instrumentation used for board testing – PXI Instrumentation – Integration of PXI instruments for testing

Design for testability (DFT) and Design for manufacturability (DFM) - Basics of ATPG, – Fault Models — Design considerations for edge functional test, Design considerations for Bus Cycle Signature Test, Design considerations for Boundary Scan Test, Built-in Self-Test, Modular Design– ATE for test - DFM - Manufacturing phases in industry oriented Production process – strategies – new strategy - benefits of new strategies

Reference Books:

1. *Test Engineering for Electronic Hardware – S R Sabapathi, Qmax Test Equipments P Ltd., 2011*
2. *Practical Electronic Fault Finding and Troubleshooting - Robin Pain Newnes, Reed Educational and professional publishing Ltd., 1996*
3. *The Fundamentals of Digital Semiconductor Testing, Floyd, Pearson Education India, Sep-2005*
4. *Building a Successful Board Test Strategy-Stephen F Scheiber-Butterworth Heinemann*

COURSE OUTCOMES

Students are able to

CO1: Understand PCB and various manufacturing techniques.

CO2: Understand common PCB failure detection techniques.

CO3: Understand the various ATE system components.

CO4: Know different board functional test techniques.

CO5: Understand the basic considerations for design manufacturability and testability.

Course Code	**:**	**EC686**
Course Title	**:**	**Introduction to Industry 4.0 and Industrial Internet of Things**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective:

- To give the students an understanding of Industry 4.0 and Cyber security.
- To develop the skills for analyzing the industrial internet of things in industry to modify the various existing industrial systems.

COURSE CONTENT

Introduction: Sensing & actuation, Communication-Part I, Part II, Networking-Part I, Part II, Industry 4.0: Globalization and Emerging Issues, The Fourth Revolution, LEAN Production Systems, Smart and Connected Business Perspective, Smart Factories, Industry 4.0: Cyber Physical Systems and Next Generation Sensors, Collaborative Platform and Product Lifecycle Management, Augmented Reality and Virtual Reality, Artifical Intelligence, Big Data and Advanced Analysis, Cybersecurity in Industry 4.0.

Basics of Industrial IoT: Industrial Processes-Part I, Part II, Industrial Sensing & Actuation, Industrial Internet Systems, IioT - Introduction, Industrial IoT: Business Model and Referece Architecture: IioT - Business Models-Part I, Part II, IIoT Reference Architecture-Part I, Part II, Industrial IoT- Layers: IIoT Sensing-Part I, Part II, IIoT Processing-Part I, Part II, IIoT Communication-Part I.

Industrial IoT- Layers: IIoT Communication-Part II, Part III, IIoT Networking-Part I, Part II, Part III, Industrial IoT: Big Data Analytics and Software Defined Networks: IIoT Analytics - Introduction, Machine Learning and Data Science - Part I, Part II, R and Julia Programming, Data Management with Hadoop, Industrial IoT: Big Data Analytics and Software Defined Networks: SDN in IIoT-Part I, Part II, Data Center Networks, Industrial IoT: Security and Fog Computing: Cloud Computing in IIoT-Part I, Part II.

Industrial IoT: Security and Fog Computing - Fog Computing in IIoT, Security in IIoT-Part I, Part II, Industrial IoT- Application Domains: Factories and Assembly Line, Food Industry, Industrial IoT- Application Domains: Healthcare, Power Plants, Inventory Management & Quality Control, Plant Safety and Security (Including AR and VR safety applications), Facility Management, Industrial IoT- Application Domains: Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies

Case study: Milk Processing and Packaging Industries, Manufacturing Industries - Part I & II, Student Projects – Part I & II, Virtual Reality Lab, Case study - VII : Steel Technology Lab

Reference Books:

1. Alasdair Gilchrist "Industry 4.0: The Industrial Internet of Things", Apress, Springer, New York, 2016.

2. Sabina Jeschke, Christian Brecher, Houbing Song, and Danda B. Rawat "Industrial Internet of Things: Cybermanufacturing Systems" Springer International Publishing Switerland, 2017.

Course Outcomes

At the end of the course student will be able to
CO1: To understand the basic concepts of communication networking
CO2: To analyze the Business model and reference architecture
CO3: To understand the globalization and emerging issues in industrial 4.0 and artificial intelligence, big data and advanced analysis
CO4: To verify the design flow of industrial IoT
CO5: To verify the process of synthesis and post-synthesis in various applications in Industrial IoT.

Course Code	**:**	**EC687**
Course Title	**:**	**VLSI SoC Design and Applications**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Content:

Introduction to SoC Architecture & Design: Basic SoC VLSI design flow – Specifications - Architecture – High/Low Level design – RTL Coding(+Lint) – Block Verification - SoC Integration & Testing – Synthesis & Scan Insertion – Formal Verification – Layout & STA – Tapeout. Different SoC Processors and its Selection.

Memory Design, Interconnect Architectures and Bus protocols: APB, AHB, I2C, SPI & UART (open-source bus protocol manuals from internet to be used as study material)

Low Power Methods : Introduction to Low Power methods, Power switch basics, Isolation, Level shifters, Clock gating, an example showing the need for Isolation in a SoC Design.

Clock Domain Crossing & STA : Clock Domain Crossing, Reset Domain Crossing, Toggle synchronizers, Double Synchronizers, Reset Synchronizers, MTBF.

Standard cell basics, how .lib modelling is done for std cell delay & power. STA concepts, Timing verification, Configuring STA environment .

SoC Applications

Reference Books:

1. *Low Power Methodology Manual for System-on-Chip Design by David Flynn, Rob Aitken, Alan Gibbons and Kaijian Shi.*
2. *http://www.sunburst-design.com/papers/CummingsSNUG2008Boston_CDC.pdf*
3. *Static Timing Analysis for Nanometer Designs : A Practical Approach by J. Bhasker and Rakesh Chadha.*
4. *"CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Money Harris, 2015.*
5. *"Digital Integrated Circuits: A Design Perspective" by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, 2002.*

Course outcomes: At the end of the course student will be able to

CO1: Gain awareness of the System-on-Chip (SoC) design flow and current semiconductor technologies.
CO2: Demonstrate proficiency in RTL coding for SPI Protocol and employ System Verilog/UVM for thorough design verification.
CO3: Identify signals necessitating low-power cells (e.g., Level shifters, isolators) in RTL designs with Always-ON and power-gated SPI controller blocks. Conduct Design Verification to prevent "X" propagation from OFF to ON domains.
CO4: Develop the capability to detect and resolve setup/hold time violations effectively during Design Verification simulations, ensuring robust SoC designs.

Course Code	**:**	**EC688**
Course Title	**:**	**VLSI Broadband Communication Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objective :
To make the students to understand the design and performance measures concept of broadband communication circuits.

Course Content:
Introduction to broadband digital communication, Serializers and de-serializers, CMOS logic, single ended data transmission, limitations, Current mode logic-basic circuit design CML to CMOS conversion, Phase rotation and interpolation, De-skew generator design

Current mode logic-MUX, XOR, latch, Current mode logic-latch design, Current mode logic-latch characteristics, Differential pair-effect of tail node capacitance; Continuous time equalization, Continuous-time equalizer realization; replica biasing for the tail current source, Replica biasing, optimizing transmitter swing, Low pass transmission channel-Inter-symbol interference, error rate, First order channel model, ISI, jitter, eye opening

Channel characteristics -Inter-symbol interference, Crosstalk, Equalizer design, Equalizer design-minimizing the residual error, Equalization-Effect on noise and crosstalk, Trade-offs between equalization at Tx and Rx; Design of Tx equalizers, Design of Transmit equalizers using flip-flops and trans-conductors, Equalization at the receiver, Equalization at the receiver

Latch vs. amplifier; Zeros for pre- and post- cursor equalization; Echo cancellation Decision feedback equalizers-elimination of noise enhancement; Error propagation Decision feedback equalizers-bit error rate

Introduction to clock and data recovery-Frequency multiplication using a phase locked loop; Type I PLL; derivation of the phase model of the PLL; Tri state phase detector; Reference feedthrough; Trade-off between reference feedthrough and lock range; Stability of feedback loops; Derivation of the type II PLL; Realization of type II PLLs-charge pump, loop filter; Reference feedthrough in a type II PLL; Phase detector for random data; Linear phase detector for random data; Transfer functions in a PLL; Binary phase detectors; bang bang jitter; Linearity assumption of PLL model; PLL capture phenomenon; Hogge phase detector offset correction

Reference Books:

1. David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 1997.
2. B. Razavi, "Principles of Data Conversion System Design", Wiley-IEEE Press, 1St Edition, 1994.
3. R. J. Baker, "CMOS Mixed Signal circuit Design", Wiley-IEEE Press, 2nd Edition, 2008.
4. M.Gustavsson, J. J. Wikner, and N. N. Tan, "CMOS Data Conversion for Communications", Springer; 2000

Course outcomes: At the end of the course student will be able to
CO1: understand the importance and the design principles of CML and CMOS logic high speed circuits
CO2: apply the high speed circuit design techniques to build equalizers and SERDES building blocks
CO3: differentiate between various trade-offs and methods of equalization
CO4: understand the nature and importance of ISI and BER in high-speed, broad-band communication circuits
CO5: Understand, design and implement Type I and Type II PLL topologies and their constituent blocks.

Course Code	**:**	**EC689**
Course Title	**:**	**High Performance Frequency Synthesizers**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand and design fully integrated, low phase noise, frequency synthesizers.
- To understand the design challenges of high performance frequency synthesizers and oscillators.

Course Content

CMOS Analog/RF components: BJT and MOSFETs (small signal model and parameters, high frequency effects, f_T, f_{max}, and noise), POLY and diffusion resistors, sheet resistance and skin effects, Metal-Insulator-Metal capacitors and varactors, on-chip Inductors, Quality factor and self-resonance, loss mechanisms and narrow-band equivalent circuit model, characterization of on chip inductors, patterned ground shields, multi-level Inductors, and Transformers.

Voltage controlled oscillators (VCO): performance parameters, oscillator closed loop analysis and negative resistance generated by amplifiers, NMOS and PMOS cross coupled LC oscillators, complementary LC oscillators, voltage limited and current limited operation, VCO tuning range and small signal model, phase noise, linear or additive phase noise models, phase noise to timing jitter conversion, design analysis and methodology for low noise oscillators, and ring oscillators.

Integer-N frequency synthesizers: Reference clock and phase detector, Type-I PLLs, transfer function and loop dynamics, Type-II PLLs, phase frequency detectors (PFD), charge-pump (CP), transfer function and loop dynamics, transient response, PFD-CP non-idealities, charge-pump circuit techniques, PLL phase noise contributors and closed loop analysis, loop bandwidth, design procedure, reference spur and reduction techniques, PLL modulation techniques.

Fractional-N frequency synthesizers: Dual modulus pre-scaler, randomization and noise shaping, fractional-N spurious components, higher order noise shaping, and 3rd order MASH sigma-delta modulator.

Course project: Design to GDS analog tapeout flow, design project involving specification to design, schematic, layout, and post-layout extraction of frequency synthesizer blocks such as PFD, charge-pump, voltage controlled LC and ring oscillators, integer-N and fractional-N divider circuits in a 65nm CMOS process.

Text Books

- *Behzad Razavi, "RF Microelectronics", Pearson Prentice Hall, 2011.*
- *Thomas H Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, 2003.*

Reference Books

- *Andrea Leonardo Lacaita, Carlo Samori, Salvatore Levantino, "Integrated Frequency Synthesizers for Wireless Systems", Cambridge University Press, 2007.*
- *John W M Rogers, and Calvin Plett, "Radio Frequency Integrated Circuit Design", Artech House Publishers, 2010.*
- *Badih El-Kareh, and Lou N. Hutter, "Silicon Analog Components- Device Design, Process Integration, Characterization, and Reliability", Springer, 2010.*

Course outcomes

At the end of the course student will be able to
CO1: understand the high frequency characteristics of on-chip analog components.
CO2: understand the basics and analyse the performance of frequency synthesizers.
CO3: appreciate the challenges involved in the design of a low noise frequency synthesizer.
CO4: design various types of synthesizers, and oscillators, and analyse their characteristics.
CO5: design high frequency on-chip circuits and systems.

Course Code	**:**	**EC 690**
Course Title	**:**	**Analog Power Integrated Circuit Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand and design power management integrated circuits such as voltage & current references, low-dropout regulators, and DC-DC converters.
- To understand the design challenges of state-of-the-art power management unit (PMU) designed for IoT and RF applications.

Course Content

Advanced design concepts: Introduction to switching and linear regulators, energy sources and load circuits, package thermal constraints, regulator performance parameters, on-chip device process variations and mismatch.

Current and voltage reference circuits: Beta multiplier current reference operating in saturation and sub-threshold region, power supply rejection ratio (PSRR) of current reference, complementary to absolute temperature (CTAT) current reference, peaking current source, temperature independent (I) reference. Bandgap voltage reference (BGR), voltage trimming, curvature correction, and PSRR improvement techniques, MOSFET only sub-threshold region based voltage reference circuits (CVR), analysis and simulation methods.

Low drop-out voltage regulators (LDO): Linear regulator, NMOS & PMOS pass-FET LDO circuits, DC and AC analysis, small signal model and stability analysis, internally and externally compensated LDOs, PSRR analysis, load & line transient analysis, and technology lookup table based LDO design methodology.

Inductive DC-DC/Switching converters: Power stage and fundamental concepts, steady state operation, volt-second balance principle, ripple current and voltage magnitude, CCM Vs DCM operation, line and load transient response, small signal model, loop gain and stability analysis, dominant pole (type-I), type-II, and type-III compensation, power-FET loss components and optimal sizing methodology, DC-DC converter loss components and efficiency calculation, DCM mode buck, boost, and buck-boost converter design, time based DC-DC controller.

Course project: Design to GDS analog tapeout flow, design project involving specification to design, schematic, layout, and post-layout extraction of voltage and current reference circuits, LDO, power-FET and DC-DC converters in a 65nm CMOS process.

Text Books

- *Bernhard Wicht, "Design of Power Management Integrated Circuits", Wiley-IEEE Press, 2024.*
- *Ke-Horng Chen, "Power Management Techniques for Integrated Circuit Design", Wiley-IEEE Press, 2016.*

Reference Books

- *Mona M. Hella, Patrick Mercier, "Power Management Integrated Circuits", CRC Press, 2016.*
- *"Power Topologies Handbook", Texas Instruments.*

Course outcomes

At the end of the course student will be able to

CO1: understand the power management unit specifications for given target applications.

CO2: understand and analyse the performance of power management integrated circuits.
CO3: appreciate the challenges involved in the design of a high performance PMU design.
CO4: design various types of voltage & current references, LDO's, and DC-DC converters.
CO5: design high efficiency on-chip power management circuits.

NPTEL Courses

Course Code	**:**	**EC801**
Course Title	**:**	**Fundamentals of MIMO Wireless Communications**
Number of Credits	**:**	**3**
Course Type	**:**	**Online Course**

Course Objective:
To introduce students to the fundamentals of multiple antenna communication

Course Content:

Evolution of wireless system, Layered view of Transmitter and Receiver, Large scale propagation models, Path loss, Shadowing, Small scale model.

Coherence time, Doppler spectrum, Flat fading, Frequency selective fading, Coherence bandwidth, Delay Doppler characteristics

MIMO Channel, Statistical Properties, Maximal Ratio Combining, Selective Combining, Spatial Diversity, Probability of error in multiple antenna systems, Diversity gain, Transmit diversity.

Fundamentals of Information Theory, Entropy, Capacity, Source Coding, Huffman theorem

Capacity of deterministic MIMO channels, Capacity of channel unknown at transmitter, Capacity of channel known at transmitter, Capacity of random channel

Text books:

1. Principles of Mobile Communications by G. Stuber, Springer, 2nd ed..
2. Wireless Communications by A. Goldsmith, Cambridge

Reference Books:

1. Introduction to Space Time Wireless Communications by A. Paulraj, Nabar and Gore
2. Space Time Wireless Communication Systems,by Bolskei, Gesbert, et al.
3. MIMO wireless communications, by Biligeri, et al.
4. Space Time Coding, by Jafarkhani
5. LTE, UMTS and The Long Term Evolution by Sesia, Toufik and Baker
6. OFDM for Wireless Communications by R. Prasad
7. UMTS for LTE by Holma and Toshala
8. Adaptive PHY-MAC Design for Broadband Wireless Systems by R. Prasad, S. S. Das and Rahman
9. Single and Multi Carrier MIMO Transmission for Broadband Wireless Systems by R. Prasad, Rahman and S. S. Das.

Course Outcomes:

CO1: Students will learn about the evolution of wireless systems.
CO2: Students will learn about the basics of wireless channels.
CO3: Students will learn about receive and transmit diversity schemes in MIMO.
CO4: Students will learn to apply information theoretic concepts in a wireless system.
CO5: Students will learn to derive the capacity of wireless systems under different scenarios.

Course Code	**:**	**EC802**
Course Title	**:**	**Evolution of Air Interface Towards 5G**
Number of Credits	**:**	**3**
Course Type	**:**	**Online Course**

Course Objective:

This course will prepare students for research and make them industry ready to work in 5G technology.

Course Content:

Overview of 5G communication technology, Introduction to mm wave, Propagation models,

Introduction to MIMO, W-OFDM, F-OFDM, UFMC, FBMC, GFDM, adaptive OFDM, Modulation and coding in 5G

Propagation characteristics of 5G channel models, Basics of MIMO, Massive MIMO, Pilot contamination, Beamforming

Heterogeneous ultra dense networks, Femtocells, Small cells, Device-to-device

Non-orthogonal-multiple access, MIMO-NOMA, QoS provisioning for real time traffic.

Textbooks:

1.Evolution of Air Interface for 5G, River Publishers 2018, Journal and conference papers, white papers.
2. “5G NR: The Next Generation Wireless Access Technology”, Erik Dahlman, Stefan parkvall, Johan Skold, Elsevier, 2E, 2020

Course Outcomes:

CO1: Students will learn about the development of 5G technology.
CO2: Students will learn about various waveforms used in 5G.
CO3: Students will learn about MASSIVE MIMO and the technologies associated with it.
CO4: Students will learn about heterogeneous networks.
CO5: Students will learn about non orthogonal multiple access.

Course Code	**:**	**EC803**
Course Title	**:**	**Introduction to Industry 4.0 and Industrial Internet of Things**
Number of Credits	**:**	**3**
Course Type	**:**	**Online Course**

Course Objective:

•To get the understanding on the foundational concepts of Industry 4.0 and the Industrial Internet of Things (IIoT) for practical applications across industries.

•To get an understanding on the IIoT enabling technologies such as Big Data Analytics, Fog computing and Software Defined Networks (SDN), and strategic considerations for potential application domains.

Course Content:

Introduction: Sensing & actuation, Communication and Networking
Industry 4.0: Globalization and Emerging Issues, The Fourth Revolution, LEAN Production Systems, Smart and Connected Business Perspective, Smart Factories. Industry 4.0: Cyber Physical Systems and Next Generation Sensors, Collaborative Platform and Product Lifecycle Management, Augmented Reality and Virtual Reality, Artificial Intelligence, Big Data and Advanced Analysis.
Cybersecurity in Industry 4.0, Basics of Industrial IoT: Industrial Processes,Industrial Sensing & Actuation, Industrial Internet Systems.

IIoT-Introduction, Industrial IoT: Business Model and Reference Architecture: IIoT-Business Models, IIoT Reference Architecture,. Industrial IoT- Layers: IIoT Sensing, IIoT Processing, IIoT Communication, Industrial IoT- Layers: IIoT Communication, IIoT Networking

Industrial IoT: Big Data Analytics and Software Defined Networks: IIoT Analytics - Introduction, Machine Learning and Data Science , R and Julia Programming, Data Management with Hadoop. Industrial IoT: Big Data Analytics and Software Defined Networks: SDN in IIoT, Data Center Networks, Industrial IoT: Security and Fog Computing: Cloud Computing in IIoT,, ParIndustrial IoT: Security and Fog Computing - Fog Computing in IIoT, Security in IIoT

Industrial IoT- Application Domains: Factories and Assembly Line, Food Industry. Industrial IoT- Application Domains: Healthcare, Power Plants, Inventory Management & Quality Control, Plant Safety and Security (Including AR and VR safety applications), Facility Management.

Industrial IoT- Application Domains: Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies:
Case study - I: Milk Processing and Packaging Industries
Case study - II: Manufacturing Industries - Part I
Case study - III: Manufacturing Industries - Part II
Case study - IV: Student Projects - Part I
Case study - V: Student Projects - Part II
Case study - VI: Virtual Reality Lab
Case study - VII: Steel Technology Lab

Textbooks:

1.S. Misra, A. Mukherjee, and A. Roy, 2020. Introduction to IoT. Cambridge University Press.
2. S. Misra, C. Roy, and A. Mukherjee, 2020. Introduction to Industrial Internet of Things and Industry 4.0. CRC Press.
3. Research Papers

Course Outcomes:

At the end of the course student will be able

CO1: Understand the development towards emergence of Industry 4.0

CO2: Learn the basic concepts of Industry 4.0

CO3: Learn the networking and communication concepts behind Industrial Internet of Things

CO4: Examine the technologies driving the Industrial Internet of Things (IIoT)

CO5: Investigate case studies and practical examples where Industry 4.0 and IIoT technologies have been successfully deployed

Course Code	**:**	**EC804**
Course Title	**:**	**VLSI Data Conversion Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand sampling and quantization in time and frequency domains, reduction of quantization noise by oversampling and noise shaping concepts.
- To design discrete-time and continuous-time Delta Sigma modulators, Flash A/D converter-Sample and hold circuits, preamplifiers and latches, D/A converter-Current Steering.

Course Content

Course overview and introduction. Sampling, Spectral properties of sampled signals, Oversampling and its implications on anti-alias filter design. Time Interleaved Sampling, Analysis of a Ping-Pong Sampling system. Ping-pong Sample and Holds continued, Analysis of Offset and Gain Errors in Time-Interleaved Sample and Holds. Sampling Circuits (NMOS, PMOS and CMOS Switches), Distortion due to the Sampling Switch. Thermal Noise in Sample and Holds, Charge Injection in a Sampling Switch.

Bottom Plate Sampling, The Gate Bootstrapped Switch. The Gate Bootstrapped Switch, the Nakagome Charge-Pump. Characterizing a Sample-and-Hold, Correct choice of input frequency, Discrete Fourier Series Refresher. FFT Leakage and the Rectangular Window. FFT Leakage, Spectral Windows, the Hann Window. Spectral Windows, the Blackman Window, Introduction to Switch Capacitor Amplifiers. Switch Capacitor Circuits, Parasitic Insensitive SC Amplifiers. Nonidealities in SC Amplifiers - Finite Opamp Gain and DC Offset, Finite Opamp Gain-Bandwidth Product.

Introduction to Fully Differential Operation. Fully-differential operation, motivation for common-mode feedback. Fully Differential SC-circuits, the "Flip-Around" Sample and Hold, DC Negative Feedback in SC Circuits. ADC Terminology, Offset and Gain Error, Differential Nonlinearity (DNL). Integral Nonlinearity (INL), Dynamic Characterization of ADCs, SQNR, Quantization Noise Spectrum. Quantization Noise Spectrum (contd), SFDR, Flash A/D Converter Basics.

Flash A/D Converter Basics, the Regenerative Latch. The Regenerative Latch. Motivation to use a Preamp, Preamp Offset Correction (Autozeroing). Autozeroing a Differential Preamp, Subtracting References from the Input. Coupling Capacitor Considerations in an Autozeroed Preamp. Transistor Level Preamp Design. Necessity of an up-front sample and hold for good dynamic performance. Timing issues in a flash ADC. Bubble Correction Logic in a Flash ADC, Comparator Metastability, Case Study. Flash ADC Case Study.

D/A Converter Basics, INL/DNL, DAC Spectra and Pulse Shapes. NRZ vs RZ DACs, DAC Architectures. Binary Weighted versus Thermometer DACs. Binary vs Thermometer DACs, Current Steering DACs. Current Steering DACs. Current Cell Design in a Current Steering DAC. Current Cell Design, Layout Considerations in Current Steering DACs.

Oversampled Approaches to Data Convresion, Benefits of Oversampling. Oversampling with Noise Shaping, Signal and Noise Transfer Functions, First and Second Order Delta-Sigma Converters. Signal Dependent Stability of DSMs, the Describing Function Method. Stability in DSMs. Maximum Stable Amplitude of DSMs and Relation to Out of Band Gain, Systematic NTF Design. Systematic NTF Design, the Bode Sensitivity Integral and its Implications on NTF Design.

Text Books

- *"CMOS Data Converters for Communication - M. Gustavsson, J. Wikner, and N. Tan. Kluwer Academic Publishers, 2000.*
- *Principles of Data Conversion System Design - Behzad Razavi.*

Reference Books

- *Delta-Sigma Data Converters: Theory, Design, and Simulation - by Steven R. Norsworthy, Richard Schreier, Gabor C. Temes (the Yellow Bible of Delta-Sigma Converters)*
- *Understanding Delta-Sigma Data Converters - by Richard Schreier, Gabor C. Temes (the Green Bible of Delta-Sigma Converters)*

Course outcomes

At the end of the course student will be able to
CO1: understand sampling concepts and design sample and hold circuits.
CO2: understand and design high performance A/D and D/A circuits.
CO3: understand non-idealities in a data conversion system.
CO4: understand advanced concepts and design methods in data conversion circuits.
CO5: understand oversample data conversion circuits.

Course Code	**:**	**EC805**
Course Title	**:**	**Introduction to Time - Varying Electrical Networks**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To introduce analog, mixed-signal and RF circuit designers to the area of time-varying circuits and systems.
- To introduces linear time-varying (LTV) and linear periodically time-varying (LPTV) circuits. The applications of the theory are illustrated with practical examples..

Course Content

Motivation for the topics covered in the course, review of linearity and time-variance; Review of electrical network basics, incidence matrix, Tellegen's theorem; Tellegen's theorem (cntd), its use to prove reciprocity in bilateral networks, reciprocity in networks with controlled sources.

Reciprocity in networks with controlled sources (contd), inter-reciprocal networks; Modified Nodal Analysis (MNA) formulation to write network equations; MNA formulation (contd), MNA stamps of circuit elements, Reciprocity and inter-reciprocity revisited, Reciprocity and inter-reciprocity (contd), the adjoint network.; Introduction to noise in electronic circuits; Noise in RLC circuits, Nyquist's theorem, Bode's Noise Theorem.

Bode's noise theorem (contd), input referred noise sources in networks; Input-referred noise sources (contd) - equivalent noise voltage and current sources; Equivalent noise sources, noise factor, Need to study time-varying circuits and systems; Linear time-varying (LTV) system basics; Linear Periodically Time-Varying (LPTV) systems basics. Harmonic transfer functions, the Zadeh expansion; MNA equations in LPTV networks with Harmonic transfer matrices; LPTV circuit example : the sampling mixer.

Impedance and admittance in LPTV networks, Norton and Thevenin equivalents; The N-path principle; N-path circuits (contd) - the time-interleaved. N-path circuits (contd) - the multiphase dc-dc converter, introduction to the N-path filter; N-path filters (contd) - input impedance and gain; N-path filters (contd). Reciprocity and inter-reciprocity in LPTV networks - time-reversal to generate the adjoint; Inter reciprocity (contd), transfer-function theorem; Inter-reciprocity (contd), the frequency-reversal theorem.

Inter-reciprocal signal-flow graphs. Example : chopped amplifiers; Chopped-amplifiers with sinusoidal and square-wave modulation; Adjoint networks - the switched-RC kernel example; time domain implications of adjoint networks. Time-domain implications of the adjoint - example of a switched-RC network. Sampled LPTV networks; Equivalent LTI filter of a sampled LPTV system; derivation of the equivalent impulse response, switched-RC network example; Cont. time delta-sigma as a sampled LPTV system. Response of LPTV systems to modulated inputs; equivalent LTI filter; Introduction to noise in LPTV networks, noise in switched-RLC networks, the Bode noise theorem applied to LPTV networks;

Text Books

- *"Engineering Circuit Analysis", William H. Hayt, Jr., Jack E. Kemmerly, Jamie D. Phillips, Steven M. Durbin, (9th edition, McGraw Hill).*
- *Alan Oppenheim, Alan Willsky, S. Nawab,"Signals and Systems", Pearson, 2006.*

Reference Books

- *Erwin Kreyszig, "Advanced Engineering Mathematics", John Willey & Sons, Inc.*
- *Dr. B.S.Grewal, "Higher Engineering Mathematics", Khanna Publishers.*

Course outcomes

At the end of the course student will be able to

CO1: understand linearity and time-variance in electrical networks.

CO2: understand reciprocity and inter-reciprocity in networks.

CO3: understand Bode's noise theorem and Linear time-varying (LTV) system.

CO4: understand impedance and admittance in LPTV networks, N-path filters.

CO5: understand inter-reciprocal signal-flow graphs and response of LPTV systems.

Course Code	**:**	**EC806**
Course Title	**:**	**Power Management Integrated Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand and design power management integrated circuits such as voltage & current references, low-dropout regulators, and DC-DC converters.
- To understand the design challenges of state-of-the-art power management unit (PMU) designed for IoT and RF applications.

Course Content

Introduction to Power Management and Voltage Regulators: Need of power management, power management applications, classification of power management, power delivery of a VLSI system, power conversion, discrete vs. integrated power management, types of voltage regulators (switching Vs linear regulators) and applications, converter's performance parameters (voltage accuracy, power conversion efficiency, load regulation, line regulation, line and load transient response, settling time, voltage tracking), local Vs remote feedback, kelvin sensing, Point-of-Load (POL) regulators.

Linear Regulators: Bandgap Voltage Reference, Low Drop-Out Regulator (LDO), Source and sink regulators, shunt regulator, pass transistor, error amplifier, small signal model and stability analysis, compensation techniques, current limiting, power supply rejection ratio (PSRR), NMOS vs. PMOS regulator, current regulator.

Switching DC-DC Converters: Types (Buck, boost, buck-boost), power FETs, choosing L and C, PWM modulation, leading, trailing and dual edge modulation, Losses in switching converters, output ripple, voltage Vs current mode control, CCM and DCM modes, hysteretic control, switched capacitor dc-dc converters, Small signal model of dc-dc converter, loop gain analysis of un-compensated dc-dc converter, type-I, type-II and type-III compensation, compensation of a voltage mode dc-dc converter, compensation of a current mode dc-dc converter, Selecting topology, selecting switching frequency and external components, sizing power FETs, segmented power FET, designing building blocks (gate driver, PWM modulator, error amplifier, oscillator, ramp generator, feedback resistors), current sensing, PFM/PSM mode for light load, effect of parasitic on reliability and performance, current limit and short circuit protection, soft start control, chip level layout and placement guidelines, board level layout guidelines, EMI considerations.

Introduction to Advanced Topics in Power Management: Digitally controlled dc-dc converters, digitally controlled LDOs, time-based control for voltage regulators, adaptive compensation, dynamic voltage scaling (DVS), Single-Inductor Multiple-Outputs (SIMO) Converters, dc-dc converters for LED lighting, Li-ion battery charger.

Text Books

- *Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer (India) Pvt. Ltd, 2005.*
- *Ke-Horng Chen, "Power Management Techniques for Integrated Circuit Design", Wiley-IEEE Press, 2016.*

Reference Books

- *Mona M. Hella, Patrick Mercier, "Power Management Integrated Circuits", CRC Press, 2016.*
- *Selected papers from IEEExplore (https://ieeexplore.ieee.org/Xplore/home.jsp).*

Course outcomes

At the end of the course student will be able to
CO1: understand the power management unit specifications for given target applications.
CO2: understand and analyse the performance of power management integrated circuits.
CO3: appreciate the challenges involved in the design of a high performance PMU design.
CO4: design various types of voltage & current references, LDO's, and DC-DC converters.
CO5: design high efficiency on-chip power management circuits.

Course Code	**:**	**EC807**
Course Title	**:**	**Optical Wireless Communications for beyond 5G Networks and IOT**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Objectives:
In this course students will be exposed to optical wireless communications for modern 5G networks and Internet of things applications

Syllabus:
Existing wireless Access Schemes, OWC/Radio Comparison, Potential OWC Application Areas, LEDs and Lasers (Internal and External Quantum Efficiency, Power and Luminous Efficiency, and Modulation Bandwidth)
PIN and APD Photodetector, Photodetection Techniques, Photodetection Noise, LOS Propagation Model, Non-LOS Propagation Model, Interference from other Light sources, Atmospheric Channel Loss, Beam Divergence, Pointing Loss, Different Atmospheric Turbulence Models

Absorption, scattering, Turbulence, Multipath interference, Physical obstruction, and Background noise, Digital Baseband Modulation Techniques like PAM, PPM, PIM etc., Multi-carrier Modulation (OFDM) for OWC, Color Shift Keying, NOMA etc.

Effect of Ambient Light Sources on Indoor OWC Link Performance, Link Performance for Multipath Propagation, FSO Link Performance under the Effect of Atmospheric turbulence, Atmospheric Turbulence-Induced Penalty and mitigation strategies

Indoor OWC link, O-OFDM and CSK Modulation Schemes, WiFi/ LiFi Co-existence, V2V Communications

References:
1."Advanced Optical Wireless Communication Systems", Shlomi Arnon, John Barry, George Karagiannidis, Robert Schober, and Murat Uysal, CAMBRIDGE UNIVERSITY PRESS
2. "Optical Wireless Communications System and Channel Modelling", Z. Ghassemlooy W. Popoola S. Rajbhandari, CRC Press

Course Outcome:
CO1: Review of basics of optical wireless communication
CO2: Expose students to photodetector performance and atmospheric effects
CO3: Expose students to different modulation techniques used in optical wireless communication
CO4: Analysis of free space optical communication
CO5: Expose students to Indoor optical wireless communication link, and advanced LiFi concepts

Course Code	**:**	**EC808**
Course Title	**:**	**5G Wireless Standard Design**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Objective:

The students normally have strong theoretical background in wireless communications systems, but negligible exposure on the use of this theory to design practical wireless systems. And current jobs in the wireless communication industry require design of standards-based practical wireless systems. The objective of this course is to bridge the gap between the theory and practise of 5G wireless communication systems, and consequently also the gap between academia and industry.

Syllabus:

Introduction, Key 5G Technologies, Adaptive Modulation and Coding, Hybrid automatic repeat request, Orthogonal frequency division multiplexing, 5G Numerology, 5G frame structure

5G physical downlink shared channel (PDSCH) transmit chain– CRC generation, 5G PDSCH transmit chain – code block segmentation, 5G PDSCH transmit chain – LDPC coding, 5G PDSCH transmit chain – rate matching, 5G PDSCH transmit chain – interleaving and concatenation

5G PDSCH transmit chain – scrambling and modulation,5G PDSCH receive chain, 5G PDSCH – map receiver design,5G baseband-RF conversion, Indigenous 5G network architecture

5G physical downlink control channel (PDCCH) transmit chain- Introduction, 5G PDCCH transmit chain – CRC and segmentation, 5G PDCCH transmit chain – Polar encoding, 5G PDCCH transmit chain – CRC Interleaver, 5G PDCCH transmit chain – sub-block interleaver, 5G PDCCH transmit chain – rate matching, 5G PDCCH transmit chain – control resource set design

5G physical uplink control channel (PUCCH), Multiple input multiple output (MIMO) transceiver chain, 5G demodulation reference signal (DM-RS) design, 5G sounding reference signal (SRS) design, 5G channel state estimation reference signal (CSI-RS), 5G MIMO codebook design, 5G FR1/FR2 design, 5G Initial Access

References:

1. *3 GPPP Standards Documents*
2. *"5G NR: The Next Generation Wireless Access Technology", Erik Dahlman, Stefan parkvall, Johan Skold, Elsevier, 2E, 2020*

Course Outcome:

CO1: Review of basics of 5G technology, numerology and frame structure
CO2: Expose students to different stages of PDSCH transmit chain
CO3: Expose students to different stages of PDCCH transmit chain
CO4: Students will learn basics of SRS, DRS, CSI-RS design
CO5: Students will get exposed to MIMO transceiver design

LIST OF OPEN ELECTIVES (Offered to MTech Communication Systems and Other Branches)

Course Code	**:**	**EC 701**
Course Title	**:**	**Frequency Synthesizer Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand and design fully integrated, low phase noise, frequency synthesizers.
- To understand the design challenges of high performance frequency synthesizers and oscillators.

Course Content

CMOS Analog/RF components: BJT and MOSFETs, POLY and diffusion resistors, sheet resistance and skin effects, Metal-Insulator-Metal capacitors and varactors, on-chip Inductors, Quality factor and self-resonance, loss mechanisms and narrow-band equivalent circuit model, and Transformers.

Voltage controlled oscillators (VCO): performance parameters, oscillator closed loop analysis and negative resistance generated by amplifiers, NMOS and PMOS cross coupled LC oscillators, complementary LC oscillators, phase noise to timing jitter conversion, and ring oscillators.

Integer-N frequency synthesizers: Reference clock and phase detector, Type-I PLLs, transfer function and loop dynamics, Type-II PLLs, phase frequency detectors (PFD), charge-pump (CP), transfer function and loop dynamics, transient response, PFD-CP non-idealities, charge-pump circuit techniques, PLL phase noise contributors and closed loop analysis, and design procedure.

Fractional-N frequency synthesizers: Dual modulus prescaler, randomization and noise shaping, fractional-N spurious components, higher order noise shaping, and 3rd order MASH sigma-delta modulator.

Course project: Design project involving specification to design, schematic, layout, and post-layout extraction of frequency synthesizer blocks such as PFD, charge-pump, voltage controlled LC and ring oscillators, integer-N and fractional-N divider circuits in a 65nm CMOS process.

Text Books

- *Behzad Razavi, "RF Microelectronics", Pearson Prentice Hall, 2011.*
- *Thomas H Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, 2003.*

Reference Books

- *Andrea Leonardo Lacaita, Carlo Samori, Salvatore Levantino, "Integrated Frequency Synthesizers for Wireless Systems", Cambridge University Press, 2007.*
- *John W M Rogers, and Calvin Plett, "Radio Frequency Integrated Circuit Design", Artech House Publishers, 2010.*
- *Badih El-Kareh, and Lou N. Hutter, "Silicon Analog Components- Device Design, Process Integration, Characterization, and Reliability", Springer, 2010.*

Course outcomes

At the end of the course student will be able to
CO1: understand the high frequency characteristics of on-chip analog components.
CO2: understand the basics and analyse the performance of frequency synthesizers.
CO3: appreciate the challenges involved in the design of a low noise frequency synthesizer.
CO4: design various types of synthesizers, and oscillators, and analyse their characteristics.
CO5: design high frequency on-chip circuits and systems.

Course Code	**:**	**EC 702**
Course Title	**:**	**Power Management Circuits**
Number of Credits	**:**	**3**
Course Type	**:**	**Elective**

Course Learning Objectives

- To understand and design power management integrated circuits such as voltage & current references, low-dropout regulators, and DC-DC converters.
- To understand the design challenges of state-of-the-art power management unit (PMU) designed for IoT and RF applications.

Course Content

Introduction to switching and linear regulators, energy sources and load circuits, package thermal constraints, regulator performance parameters, on-chip device process variations and mismatch.

Current and voltage reference circuits: Beta multiplier current reference operating in saturation and sub-threshold region, complementary to absolute temperature (CTAT) current reference, peaking current source, temperature independent (I) reference. Bandgap voltage reference (BGR), MOSFET only sub-threshold region based voltage reference circuits (CVR), analysis and simulation methods.

Low drop-out voltage regulators (LDO): Linear regulator, NMOS & PMOS pass-FET LDO circuits, DC and AC analysis, small signal model and stability analysis, internally and externally compensated LDOs, PSRR analysis, load & line transient analysis.

Inductive DC-DC/Switching converters: Power stage and fundamental concepts, steady state operation, volt-second balance principle, ripple current and voltage magnitude, CCM Vs DCM operation, line and load transient response, small signal model, loop gain and stability analysis, power-FET sizing methodology, DC-DC converter loss components and efficiency calculation, DCM mode buck, boost, and buck-boost converter design.

Course project: Design project involving specification to design, schematic, layout, and post-layout extraction of voltage and current reference circuits, LDO, power-FET and DC-DC converters in a 65nm CMOS process.

Text Books

- *Bernhard Wicht, "Design of Power Management Integrated Circuits", Wiley-IEEE Press, 2024.*
- *Ke-Horng Chen, "Power Management Techniques for Integrated Circuit Design", Wiley-IEEE Press, 2016.*

Reference Books

- *Mona M. Hella, Patrick Mercier, "Power Management Integrated Circuits", CRC Press, 2016.*
- *"Power Topologies Handbook", Texas Instruments.*
- *Selected papers from IEEExplore (https://ieeexplore.ieee.org/Xplore/home.jsp).*

Course outcomes

At the end of the course student will be able to
CO1: understand the power management unit specifications for given target applications.
CO2: understand and analyse the performance of power management integrated circuits.
CO3: appreciate the challenges involved in the design of a high performance PMU design.
CO4: design various types of voltage & current references, LDO's, and DC-DC converters.
CO5: design high efficiency on-chip power management circuits.