List of Conference

1. AT Vanaraj, R Marshal, G Lakshminarayanan, KR Sekar **"Optimal test scenarios based regression suite for functional verification closure of advanced digital designs"**, 2024 International Conference on Smart Systems for applications in Electrical Sciences (ICSSES).
2. MR PC, MR Akshayraj, VP Gopi, G Lakshminarayanan, GR Gangadharan, **"Dynamic Precision Scaling in MAC Units for Energy-Efficient Computations in Deep Neural Network Accelerators"**,2024 28th International Symposium on VLSI Design and Test (VDAT), 1-7
3. MR Akshayraj, MR PC, VP Gopi, G Lakshminarayanan, GR Gangadharan, **"Energy-Efficient Hardware Design for CNN-Based ECG Signal Classification in Wearable Bio-Medical Devices"**,2024 28th International Symposium on VLSI Design and Test (VDAT), 1-7
4. K Ranjit Kannan, G Lakshminarayanan, **"Novel Approach for the Reduction of Critical Paths in Static Timing Analysis Without Degradation in QOR"**, Emerging Electronic Devices, Circuits and Systems: Select Proceedings of EEDCS workshop held in conjunction with ISDCS.
5. AT Vanaraj, R Marshal, G Lakshminarayanan, A Venkitachalam, "**Area Efficient Reliable QCA Adder and Subtractor"**, 2023 IEEE International Conference on Integrated Circuits and Communication Systems (ICICACS).
6. AT Vanaraj, KR Sekar, R Marshal, A Venkitachalam, **"Reliable Quantum-dot Cellular Automata Coplanar Adder and Subtractor for Multi-bit Designs"**,2022 13th International Conference on Computing Communication and Networking Technologies (ICCCNT).
7. AT Vanaraj, R Marshal, G Lakshminarayanan, **"Optimal Test Sequences for Logic Verification closure in State Dependent**

RTL Digital designs",2022 13th International Conference on Computing Communication and Networking Technologies (ICCCNT).

8. AT Vanaraj, M Raj, L Gopalakrishnan**, "Energy-efficient coplanar adder and subtractor in QCA"**, 2020 Third International Conference on Smart Systems and Inventive Technology (ICSSIT).
9. AT Vanaraj, M Raj, L Gopalakrishnan, **"Functional verification closure using optimal test scenarios for digital designs"**, 2020 Third International Conference on Smart Systems and Inventive(ICSSIT).
10. M Raj, L Gopalakrishnan, **"Cost Efficient Subtractor Designs in QCA"** 2020 International Conference on Electronics and Sustainable Communication Systems (ICESC).
11. RS Kumaresan, M Raj, L Gopalakrishnan, **"Area-efficient D-flip flop and XOR in QCA"**, 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT).
12. P Kumar, CM Ananda, G Lakshminarayanan, **"Design Approach for FPGA based High Bandwidth Fibre Channel Analyser for Aerospace Application"**, 2019 4th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT).
13. M Raj, RS Kumaresan, L Gopalakrishnan, **"Optimized Multiplexer and Exor gate in 4-dot 2-electron QCA using Novel Input Technique"**, 2019 10th International Conference on Computing, Communication and Networking Technologies (ICCCNT).
14. M Raj, RS Kumaresan, L Gopalakrishnan, **"High speed controllable inverter for adder-subtractor in QCA"**, 2019 10th International Conference on Computing, Communication and Networking Technologies (ICCCNT).
15. M Raj, L Gopalakrishnan**, "Novel reliable QCA subtractor designs using Clock zone-based crossover"**, 2019 3rd

International conference on Electronics, Communication and Aerospace Technology (ICECA).

16. M Raj, L Gopalakrishnan, **"Efficient quantum-dot cellular automata comparator for nanoscale communication"** 2019 TEQIP III Sponsored International Conference on Microwave Integrated Circuits, Photonics and Wireless Networks (IMICPW).
17. GS Babu, L Gopalakrishnan, **"Low-Complexity Successive Cancellation Decoder with Scan Chain"** 2018 International Conference on Circuits and Systems in Digital Enterprise Technology (ICCSDET).
18. A Alagarsamy, L Gopalakrishnan, **"Mba: a new cluster based bandwidth and power aware mapping for 2d noc"**, 2018 International Conference on Circuits and Systems in Digital Enterprise Technology (ICCSDET).
19. M Raj, L Gopalakrishnan, **"Design and defect analysis of novel NAND/NOR gate in quantum-dot cellular automata"**, 2018 International Conference on Circuits and Systems in Digital Enterprise Technology (ICCSDET).
20. LM Sistla, G LakshmiNarayanan, **"An ASIC Implementation of Successive Cancellation Decoder with Built-In Scan Chain"**, 2018 International Conference on Recent Innovations in Electrical, Electronics & Communication Engineering (ICRIEECE).
21. K Dubey, R Marshal, G Lakshminarayanan**, "Design of majority logic based comparator"**, 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT).
22. P Ishwerya, S Geethu, G Lakshminarayanan**, "An efficient hybrid spectrum sensing architecture on FPGA"** 2017 International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET).
23. P Ishwerya, S Geethu, G Lakshminarayanan, **"Autocorrelation based spectrum sensing architecture on FPGA with dynamic offset compensation"**, 2016 IEEE

Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER).

24. P Ishwerya, VN Kumar, G Lakshminarayanan, **"An efficient digital baseband encoder for short range wireless communication applications"**, 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT).
25. KB Jaiswal, N Kumar, P Seshadri, G Lakshminarayanan, **"Low power wallace tree multiplier using modified full adder"**, 2015 3rd international conference on signal processing, communication and networking (ICSCN).
26. VN Kumar, KR Nalluri, G Lakshminarayanan, **"Design of area and power efficient digital FIR filter using modified MAC unit"**, 2015 2nd International Conference on Electronics and Communication Systems (ICECS).
27. BNG Koneru, VKT Mantripragada, PR Pani, G Lakshminarayanan, **"Novel Design and Implementation of Passive Infrared Sensor in Steel Industry Automation"**, Intelligent Computing and Applications: Proceedings of the International Conference on ICA, 22-24 December 2014.
28. AX Glittas, G Lakshminarayanan, **"Pipelined FFT architectures for real-time signal processing and wireless communication applications"**, 18th International Symposium on VLSI Design and Test, 1-2.
29. K Swaminathan, S Gopi, G Lakshminarayanan, SB Ko, **"A novel hybrid topology for Network on Chip"**, 2014 IEEE 27th Canadian Conference on Electrical and Computer Engineering (CCECE).
30. SG Nambiar, K Swaminathan, G Lakshminarayanan, SB Ko**, "QaMC-QoS Aware Multicast router for NoC fabric"** 2014 IEEE 27th Canadian Conference on Electrical and Computer Engineering (CCECE).
31. K Swaminathan, D Thakyal, SG Nambiar, G Lakshminarayanan, SB Ko, **"Enhanced Noxim simulator for performance evaluation of network on chip topologies"** 2014

Recent Advances in Engineering and Computational Sciences (RAECS), 1-5.

32. SG Nambiar, K Swaminathan, G Lakshminarayanan, SB Ko, **"Central Switch Noded Mesh architecture (CSNM)"**, 2014 International Conference on Electronics and Communication Systems (ICECS).

33. VN Kumar, H Bhalavi, G Lakshminarayanan, M Sellathurai, **"FPGA based decision making engine for cognitive radio using genetic algorithm"**, 2013 IEEE 8th International Conference on Industrial and Information Systems.

34. VN Kumar, KV Reddy, S Geethu, G Lakshminarayanan, M Sellathurai, **"Reconfigurable hybrid spectrum sensing technique for cognitive radio"**, 2013 IEEE 8th International Conference on Industrial and Information Systems.

35. C Vennila, K Suresh, R Rather, G Lakshminarayanan, **"Dynamic partial reconfigurable adaptive transceiver for OFDM based cognitive radio"**, 2013 26th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).

36. K Swaminathan, G Lakshminarayanan, F Lang, M Fahmi, SB Ko, **"Design of a low power network interface for Network on chip"** 2013 26th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).

37. K Swaminathan, G Lakshminarayanan, SB Ko, **"High speed generic network interface for network on chip using ping pong buffers"**, 2012 International Symposium on Electronic System Design (ISED), 72-76.

38. S Geethu, GL Narayanan**, "A novel selection based hybrid spectrum sensing technique for cognitive radios"**, 2012 2nd International conference on power, control and embedded systems, 1-6.

39. C Vennila, KP CT, KV Krishna, G Lakshminarayanan, SB Ko, **"Dynamic partial reconfigurable FFT/IFFT pruning for OFDM based Cognitive radio"**, 2012 IEEE International Symposium on Circuits and Systems (ISCAS), 33-36.

40. DN Sarma, G Lakshminarayanan, KVRS Chavali, **"A Novel Encoding Scheme for Low Power in Network on Chip Links"**, 2012 25th International Conference on VLSI Design, 257-261.
41. DN Sarma, G Lakshminarayanan**, "Encoding technique for reducing power dissipation in network on chip serial links"**, 2011 International Conference on Computational Intelligence and Communication Networks.
42. CV Arasu, S Nagrale, G Lakshminarayanan, **"FPGA implementation of adaptive mode PAPR reduction for cognitive radio applications"**, 2011 International Conference on Communication Systems and Network Technologies.
43. CV Arasu, P Hyanki, HL Sharma, G Lakshminarayanan, MH Lee, SB Ko, **"PAPR reduction for improving performance of OFDM system"**, 2010 International Conference On Communication Control and Computing Technologies.
44. M Santhi, G Seetharaman, R Silwal, G Lakshminarayanan, **"A Novel Online Clock Skew Scheme for FPGA Based Asynchronous Wave-Pipelined Circuits"** 2010 5th International Conference on Future Information Technology, 1-6.
45. C Vennila, A Krishnan, A Raj, GM Reddy, TP Santosh, VK Kumar**, "Design of self reconfigurable task scheduler to implement multi-rate MB-OFDM UWB wireless system"**, 2010 International Conference on Electronic Devices, Systems and Applications.
46. C Vennila, G Lakshminarayanan, S Tungala, **"Design of reconfigurable UWB transmitter to implement multi-rate MB-OFDM UWB wireless system"**, 2009 International Conference on Advances in Computing, Control, and Telecommunication Technologies.
47. SG Talekar, S Ramasamy, G Lakshminarayanan, B Venkataramani, **"500ms/s 4-b time interleaved sar adc using novel dac architecture"**, 2009 1st Asia Symposium on Quality Electronic Design, 292-297.

48. M Santhi, G Lakshminarayanan, C Balakrishna, S Tungala, **"Design of low power Asynchronous Pipelined Systems with Input Change Detection Circuit"**, 2009 International Conference on Control, Automation, Communication and Energy Conservation.

49. M Santhi, G Lakshminarayanan, S Tungala, C Balakrishna, **"FPGA based asynchronous pipelined OFDM for MB-OFDM UWB application"**, 2009 International Conference on Control, Automation, Communication and Energy Conservation.

50. M Santhi, S Tungala, C Balakrishna, G Lakshminarayanan, **"Asynchronous pipelined MB-OFDM UWB transceiver on FPGA"**, TENCON 2009-2009 IEEE Region 10 Conference, 1-5.

51. SG Talekar, S Ramasamy, G Lakshminarayanan, B Venkataramani, **"A low power 700msps 4bit time interleaved sar adc in 0.18 um cmos"**, TENCON 2009-2009 IEEE Region 10 Conference, 1-5.

52. T Kumaran, M Santhi, M Srikanth, N Srinivasan, M Balaji, **"Transient current sensing based completion detection with event separation logic for high speed asynchronous pipelines"**, TENCON 2009-2009 IEEE Region 10 Conference, 1-6.

53. M Santhi, MS Kumar, G Lakshminarayanan, TN Prabakar, **"Design and implementation of pipelined MB-OFDM UWB transmitter backend modules on FPGA"**, 2008 International Conference on Computing, Communication and Networking, 1-6.

54. TN Prabakar, G Lakshminarayanan, KK Anilkumar, **"FPGA based asynchronous pipelined multiplier with intelligent delay controller"**, 2008 International SoC Design Conference 1, I-304-I-309.

55. M Santhi, G Lakshminarayanan, SV Varadhan, **"FPGA based asynchronous pipelined viterbi decoder using two phase bundled-data protocol"**, 2008 International SoC Design Conference 1, I-314-I-317.

56. TN Prabakar, G Lakshminarayanan, KK Anilkumar, **"SOPC based asynchronous pipelined DCT with self-test capability"**, 2007 International Conference on Microelectronics, 65-68.

57. G Lakshminarayanan, TN Prabakar, **"On-Board Verification of FPGA Based Digital Systems using NIOS Processor (A Methodology Without Hook-Ups and I/O Cards)"**, 2007 International Conference on Signal Processing, Communications and Networking.
58. G Lakshminarayanan, TN Prabakar, **"Design & implementation of asynchronous braun array multiplier"** International Conference on Advanced Computing and communication, 61-66.
59. G Lakshminarayanan, TN Prabakar, **"On board testing of digital systems using nios processor"**, IEEE International Conference on Signal Conditioning & Networking, 295-297.
60. G Seetharaman, B Venkataramani, G Lakshminarayanan, **"Design and FPGA implementation of lifting scheme for 2DDWT using wavepipelining"**, Proceedings of the 5th WSEAS International Conference on Signal Processing, Computational Geometry & Artificial Vision.
61. G Lakshminarayanan, B Venkataramani, JS Kumar, AK Yousuf, G Sriram, **"Design and FPGA implementation of image block encoders with 2D-DWT"**, TENCON 2003. Conference on Convergent Technologies for Asia-Pacific Region, Volume:3.
62. G Lakshminarayanan, B Venkataramani, KP Senthilkumar, M Kottapalli, **"Design and implementation of FPGA based wavepipelined fast convolver"**, 2000 TENCON Proceedings. Intelligent Systems and Technologies for the New Millennium (Cat. No. 00CH37119).
63. G Lakshminarayanan, B George, B Venkataramani, A Ramakalyan, **"Neural network controlled shift register traffic shaper for ATM networks"**, Proceedings of IEEE TENCON'98. IEEE Region 10 International Conference on Global Connectivity in Energy, Computer, Communication and Control (Cat. No. 98CH36229).