

List of Publications – Journals

1. TS Manivannan, KR Pasupathy, G Lakshminarayanan, “**Ambipolar current suppression in drain elevated TFET using a novel extended drain structure with a moderate doping profile**”, Microelectronics Journal 151, 106302.
2. TS Manivannan, KR Pasupathy, MRU Shaikh, G Lakshminarayanan, “**Optimization of DE-QG TFET using novel CIP and DCT techniques**”, Microelectronics Journal 144, 106097.
3. R Marshal, K Raja Sekar, L Gopalakrishnan, AT Vanaraj, SB Ko, “**Designing Fault-Tolerant Digital Circuits in Quantum-Dot Cellular Automata**”, Design and Applications of Emerging Computer Systems, 671-686.
4. L Gopalakrishnan, SB Ko, “**EMSOA based application mapping framework for power optimisation in 3D-NoC**”, International Journal of Electronics 111 (1), 149-169,2024.
5. L Gopalakrishnan, AT Vanaraj, “**8 Physically Realizable Reversible Logic Gates**” Quantum-Dot Cellular Automata Circuits for Nanocomputing Applications, 185.
6. L Gopalakrishnan, SB Ko, “**Multiobjective piecewise regressive elitism spotted hyena optimized mapping for 3D NoC architecture design**”, International Journal of Information Technology 15 (5), 2719-2728
7. RS Kumaresan, M Raj, L Gopalakrishnan, “**Framework for QCA layout generation and rules for rotated cell design**”, Journal of Circuits, Systems and Computers 32 (07), 2350114.
8. A Alagarsamy, S Mahilmaran, L Gopalakrishnan, SB Ko, “**SaHNoC: an optimal energy efficient hybrid networks-on-chip architecture**”, The Journal of Supercomputing 79 (6), 6538-6559.
9. R Marshal, G Lakshminarayanan, “**Fault resistant coplanar QCA full adder-subtractor using clock zone-based crossover**”, IETE Journal of Research 69 (1), 584-591
10. P Ramalingam, R Thanuja, R Bhavani, L Gopalakrishnan, “**An efficient lossless telemetry data compression and fault analysis system using 2SMLZ and CMOW-DLNN**”, Wireless Personal Communications 127 (3), 2325-2345.
11. A Alagarsamy, S Mahilmaran, L Gopalakrishnan, SB Ko, “**FRDS: An efficient unique on-Chip interconnection network architecture**”, Integration 87, 90-103.
12. A Alagarsamy, S Mahilmaran, L Gopalakrishnan, SB Ko, “**SMA: A constructive partitioning based mapping approach for Networks-on-Chip**”, Microprocessors and Microsystems 94, 104678.

13. U Tiwari, S Vollala, N Ramasubramanian, BS Begum, “**Secure and energy efficient design of multi-modular exponential techniques for public-key cryptosystem**”, Journal of Communications and Information Networks 7 (3), 309-323.
14. G SUSHMA, L Gopalakrishnan, SBUM KO, “**Pareto technique optimization for 3D NOC architecture**”, Research Square, <https://doi.org/10.21203/rs.3.rs-1977082/v1>.
15. KR Sekar, R Marshal, G Lakshminarayanan, “**Reliable adder and multipliers in QCA technology**”, Semiconductor Science and Technology 37 (9), 095006.
16. SR James, L Gopalakrishnan, “**Successive cancellation decoding of polar codes using new hybrid processing element**”, International Journal of Reconfigurable and Embedded Systems 11 (2), 157.
17. G Lakshminarayanan, “**Low Power, Area Efficient Architecture for Successive Cancellation Decoder**”, EMITTER International Journal of Engineering Technology, 170-182.
18. M Raj, KR Sekar, G Lakshminarayanan, “**Majority-Logic-Based Self-Checking Adder in Quantum-Dot Cellular Automata**”, IEEE Design & Test 39 (5), 88-97.
19. RS Kumaresan, M Raj, L Gopalakrishnan, “**Design and implementation of a nano magnetic logic barrel shifter using beyond-CMOS technology**”, Journal of Electrical Engineering 73 (1), 1-10.
20. G Sushma, A Alagarsamy, L Gopalakrishnan, AR Vadde, “**Multicriteria Deming Regressive African Buffalo Optimized Mapping for 3D NoC Architecture Design**”, Mathematical Problems in Engineering 2022
21. P Ramalingam, L Gopalakrishnan, M Ramachandran, R Patan, “**Kinematic adaptive frequency sampling combined spatio temporal features for snow monitoring in aerospace applications**”, Expert Systems with Applications 184, 115472.
22. KR Sekar, R Marshal, G Lakshminarayanan, “**High-speed serial–parallel multiplier in quantum-dot cellular automata**”, IEEE Embedded Systems Letters 14 (1), 31-34.
23. M Raj, L Gopalakrishnan, SB Ko, “**Design and analysis of novel QCA full adder-subtractor**”, International Journal of Electronics Letters 9 (3), 287-300.
24. M Raj, L Gopalakrishnan, SB Ko, “**Reliable SRAM using NAND-NOR gate in beyond-CMOS QCA technology**” IET Computers & Digital Techniques 15 (3), 202-213
25. M Asadikouhanjani, H Zhang, L Gopalakrishnan, HJ Lee, SB Ko, “**A real-time architecture for pruning the effectual computations in deep neural networks**”, IEEE Transactions on Circuits and Systems I: Regular Papers 68 (5), 2030-2041.
26. KR Pasupathy, TS Manivannan, G Lakshminarayanan, “**A review of engineering techniques to suppress ambipolarity in tunnel FET**”, Silicon 14 (5), 1887-1894

27. Umamaheswaran, R., Ramalingam, P., Raj, M., Gopalakrishnan, “**A Novel Boundary Elemental Analysis Based Frequency Domain Adaptive Sampling Technique for Aerospace Application**”, *Microprocessors and Microsystems* 83.
28. AX Glittas, L Gopalakrishnan, “**A low latency modular-level deeply integrated MFCC feature extraction architecture for speech recognition**”, *Integration* 76,69-75
29. JS Roy, G Lakshminarayanan, SB Ko, “**High-speed architecture for successive cancellation decoder with split-g node block**”, *IEEE Embedded Systems Letters* 13 (3), 118-121
30. AXGX Chelliah, BPS Robinson, M Sellathurai, L Gopalakrishnan, “**A power-efficient variable-length prime factor MDC FFT architecture for high-speed wireless communication applications**”, *AEU-International Journal of Electronics and Communications* 120, 153194.
31. AX Glittas, M Sellathurai, G Lakshminarayanan, “**Reconfigurable 2, 3 and 5-point DFT processing element for SDF FFT architecture using fast cyclic convolution algorithm**” *Electronics Letters* 56 (12), 592-594.
32. AT Vanaraj, M Raj, L Gopalakrishnan, “**Reliable coplanar full adder in quantum-dot cellular automata using five-input majority logic**”, *Journal of nanophotonics* 14 (2), 026017-026017
33. M Raj, S Ahmed, L Gopalakrishnan, “**Subtractor circuits using different wire crossing techniques in quantum-dot cellular automata**”, *Journal of nanophotonics* 14 (2), 026007-026007.
34. M Raj, L Gopalakrishnan, SB Ko, N Naganathan, N Ramasubramanian, “**Configurable logic blocks and memory blocks for beyond-CMOS FPGA-based embedded systems**”, *IEEE Embedded Systems Letters* 12 (4), 113-116.
35. RM R. Umamaheswaran, S.R. Santhosh Kumaran, R. Parameshwaran, G , “**An Optimized VLSI Based High Performance Architecture for Lossless Data Compression**” *International Journal of Advanced Science and Technology*, 9503-10
36. M Raj, L Gopalakrishnan, “**Cost-efficient full adder designs in quantum-dot cellular automata**”, *International Journal of Materials and Product Technology* 61 (1), 1-15.
37. M Raj, L Gopalakrishnan, “**Cost-efficient fast adder in quantum-dot cellular automata**”, *Journal of nanophotonics* 13 (4), 046012-046012.
38. M Raj, L Gopalakrishnan, SB Ko, “**Fast quantum-dot cellular automata adder/subtractor using novel fault tolerant exclusive-or gate and full adder**”, *International Journal of Theoretical Physics* 58, 3049-3064.

39. A Alagarsamy, L Gopalakrishnan, SB Ko, “**KBMA: A knowledge-based multi-objective application mapping approach for 3D NoC**”, IET Computers & Digital Techniques 13 (4), 324-334.
40. A Alagarsamy, L Gopalakrishnan, S Mahilmaran, SB Ko, “**A self-adaptive mapping approach for network on chip with low power consumption**”, IEEE Access 7, 84066-84081
41. GS Babu, LR Madala, L Gopalakrishnan, M Sellathurai, “**Low-complex processing element architecture for successive cancellation decoder**” Integration 66, 80-87
42. GS Babu, L Gopalakrishnan, “**Reconfigurable address generator for multi-standard interleaver**”, Microprocessors and Microsystems 65, 47-56.
43. S Salini, A Aravindhan, G Lakshminarayanan, “**A case study on cluster based power aware mapping strategy for 2D NoC**”, ICTCAT J. Microelectron 2 (4), 315-322.
44. A Xavier Glittas, M Sellathurai, G Lakshminarayanan, “**Two-parallel pipelined fast Fourier transform processors for real-valued signals**”, IET Circuits, Devices & Systems 10 (4), 330-336.
45. NK Venkatachalam, L Gopalakrishnan, M Sellathurai, “**Low complexity and area efficient reconfigurable multimode interleaver address generator for multistandard radios**”, IET Computers & Digital Techniques 10 (2), 59-68.
46. AX Glittas, M Sellathurai, G Lakshminarayanan, “**A normal I/O order radix-2 FFT architecture to process twin data streams for MIMO**”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24 (6 ...
47. A Aravindhan, S Salini, G Lakshminarayanan, “**Cluster based application mapping strategy for 2D NoC**”, Procedia Technology 25, 505-512.
48. VN Kumar, KR Nalluri, G Lakshminarayanan, M Sellathurai, “**An Improved Reconfigurable Finite Impulse Response Filter Using Common Subexpression Elimination Algorithm for Cognitive Radio**”, Journal of Low Power Electronics 11 (2), 181-189.
49. VN Kumar, PP Raj, G Lakshminarayanan, M Sellathurai, “**Low power and area efficient carry select adder**”, Journal of Low Power Electronics 10 (4), 593-601.
50. K Swaminathan, G Lakshminarayanan, SB Ko, “**Design and verification of an efficient WISHBONE-based network interface for network on chip**”, Computers & Electrical Engineering 40 (6), 1838-1857.
51. K Swaminathan, G Lakshminarayanan, SB Ko, “**High speed low power ping pong buffering based network interface for network on chip**”, Journal of Low Power Electronics 9 (3), 322-331.

52. C Vennila, AK Patel, G Lakshminarayanan, SB Ko, “**Dynamic partial reconfigurable Viterbi decoder for wireless standards**”, Computers & Electrical Engineering 39 (2), 164-174.
53. TN Prabakar, G Lakshminarayanan, G Seetharaman, “**Design and Implementation of SoPC based Low power Asynchronous Image Processor**”, Applied Mechanics and Materials 239, 1179-1183.
54. M Santhi, G Lakshminarayanan, B Venkataramani, “**Design and Implementation of Online Clock Skew Scheme-based Asynchronous Wave-pipelined Distributed Arithmetic Filters on FPGA**”, IETE Journal of Research 58 (6), 494-500.
55. M Santhi, S Sarangan, K Murali, G Lakshminarayanan, “**Performance analysis of pseudo 4-phase dual-rail asynchronous protocol**”, International Journal of Electronics 99 (8), 1101-1113.
56. C Vennila, G Lakshminarayanan, SB Ko, “**Dynamic partial reconfigurable FFT for OFDM based communication systems**”, Circuits, Systems, and Signal Processing 31, 1049-1066.
57. H Zhang, D Subbian, G Lakshminarayanan, SB Ko, “**Application-Specific and Reconfigurable AI Accelerator**”, Artificial Intelligence and Hardware Accelerators, 183-223.
58. S Geethu, GL Narayanan, “**A novel high speed two stage detector for spectrum sensing**”, Procedia Technology 6, 682-689.
59. TN Prabakar, G Lakshminarayanan, “**Design and Implementation of an Asynchronous Controller for FPGA Based Biosignal Processing**”, International Journal of Computer Applications 4 (4), 32-37.
60. M Santhi, G Lakshminarayanan, “**Fpga Based Asynchronous Pipelined Mb-Ofdm Uwb Transmitter Backend Modules**”, Ictact Journal of Communication Technology, 103-110.
61. TN Prabakar, G Lakshminarayanan, KK Anilkumar, “**Design and implementation of an Asynchronous Controller for FPGA Based Asynchronous Systems**”, International Journal of Computer Applications 975, 8887.
62. M Santhi, SA Kumar, GSP Kalish, S Sarangan, G Lakshminarayanan, “**A Novel Pseudo 4-Phase Dual-Rail Asynchronous Protocol with Self-Reset Logic & Multiple-Reset**”, International Journal of Computer Applications 975, 8887.
63. G Seetharaman, B Venkataramani, G Lakshminarayanan, “**Automation techniques for implementation of hybrid wave-pipelined 2D DWT**”, Journal of Real-Time Image Processing 3, 217-229.

- 64.G Seetharaman, B Venkataramani, G Lakshminarayanan, “**Design and FPGA implementation of self-tuned wave-pipelined filters with distributed arithmetic algorithm**”, Circuits, Systems & Signal Processing 27, 261-276.
- 65.G Seetharaman, B Venkataramani, G Lakshminarayanan, “**VLSI implementation of hybrid wave-pipelined 2D DWT using lifting scheme**”, VLSI Design 2008.
- 66.G Seetharaman, B Venkataramani, G Lakshminarayanan, “**Design and FPGA implementation of self tuned wavepipelined filters**”, IETE journal of research 52 (4), 281-286
- 67.G Lakshminarayanan, B Venkataramani, “**Optimization techniques for FPGA-based wave-pipelined DSP blocks**”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 13 (7), 783-793.
- 68.G Lakshminarayanan, B Venkataramani, MY Shariff, T Rajavelu, “**Self tuning circuit for FPGA based wavepipelined multipliers**”, Proc. of VLSI Design & Test Workshop VDAT04, 93-101.
- 69.R Marshal, SK Raja, L Gopalakrishnan, SB Ko, AT Vanaraj, “**Efficient layout techniques to design physically realizable quantum-dot cellular automata circuits**” Low Power Designs in Nanodevices and Circuits for Emerging Applications, 177-188.