

# National Institute of Technology, Tiruchirappalli:

## CV of Dr. B. Venkataramani/Professor, ECE

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### Curriculum Vitae



#### Brief Profile:

- Guided the projects which won first and second prize in Altera Embedded design contest in two consecutive years in 2006 and 2007.
- Awarded the best tutor award in 2007 by Altera
- Work done by me and my Ph.D. scholar G.Lakshminarayanan was awarded Indian patent.
- Executed 13 projects on VLSI (Funding in Rs. lakhs 365) as PI . 3 projects as CI (Funding in Rs. lakhs 110)
- Published 30 papers in journals and 75 papers in national/international conferences
- Authored two books
- Fabricated 4 integrated circuits
- New laboratories set up during my tenure as HOD of ECE(Electronics lab, Wireless Lab, Digital lab, Embedded system lab & VLSI lab)
- MIS for the institute was procured under my coordination. Training for all the staff was organized. The Service registers of all the staff were entered in MIS. Upgraded the features as per the user requirements.
- Set up the new labs on Atom processors and Programmable system on chip
- Guided 15 Ph.D students (8 completed + 7 ongoing) + 4 MS and 100 M.Tech thesis works
- New experiments introduced in Analog IC laboratory, Embedded system laboratory and Electronic CAD labs
- Organized workshops for the benefit of students and staff every year
- Offered internships to about 10 students every year during summer vacation.
- As nodal officer for NMEICT- NKN project, coordinated the setting up of the Virtual class room at NIT, Trichy
- As a coordinator of the Special manpower development programme for VLSI, received CAD tools worth Rs.50 lakhs and running expense of Rs.50 lakhs was sanctioned to NITT and was fully utilized
- Mentored and counseled the staff and students of ECE
- Interacted actively with alumni and arranged guest lectures at NITT periodically
- Solar powered water heaters and street lights were procured and installed by me during 2006-2009
- Prepared the Vision document on Smart campus Ventures for NIT, Trichy
- Collaborated with foreign universities such as university of Toledo, State University of Newyork, Georgia Tech for research and curriculum development
- Actively participated in syllabus revision for our department.
- Introduced and taught the upcoming topics in the syllabus: This includes software defined radio, Electronic packaging



**National Institute of Technology, Tiruchirappalli:**  
**CV of Dr. B. Venkataramani/Professor, ECE**

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8. Academic Qualifications (From Highest Degree to High School):

Examination	Board / University	Year	Division/ Grade	Subjects
Ph.D	IIT,Kanpur	1996	9.5	Queueing Analysis of a Non-preemptive MMPP/D/1/K Priority System for Applications in ATM Networks
M.Tech.	IIT,Kanpur	1984	9.75	Electrical Engineering
B.E. (Hons.)	Regional Engg. College Tiruchirappalli	<b>1979</b>	76.3	Electronics and communication

9. Academic/Administrative Responsibilities within the University

Position	Faculty/Department/Centre/Institution	From	To
Convener	Community Radio Station NITT FM 90.8	Nov 2016	Till date
Convener	Teaching Learning Centre	Sep-2015	Till date
Nodal Officer	GIAN	Sep-2015	Till date
Dean	Research & Consultancy	Sep-2012	Sept-2015
Nodal officer	NKN-NMEICT	March -2011	Till date
MIS coordinator		Dec-2007	Feb- 2011
HOD	Computer Support Group	October-1997	May-2000
HOD	Department of ECE	Dec 2007	Feb 2011
Faculty	REC,Trichy	May-1987	Till date

10. Academic/Administrative Responsibilities outside the University

Position	Institution	From	To

11. Awards, Associateships etc.

Year of Award	Name of the Award	Awarding Organization
2011	Indian Patent No. 220117	Indian Patent Office
2007	Best Tutor Award	Altera Corporation, USA

**National Institute of Technology, Tiruchirappalli:**  
**CV of Dr. B. Venkataramani/Professor, ECE**

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12. Fellowships

Year of Award	Name of the Fellowship	Awarding Organization	From (Month/Year)	To (Month/Year)

13. Details of Academic Work

(i) Curriculum Development

I proposed the M.Tech course on VLSI system in 1999 along with Prof. P. Somaskandan. Since then I have been modifying the syllabus in tune with the changes in the technology

(ii) Courses taught at Postgraduate and Undergraduate levels

UG	PG
1. VLSI Systems (UG)	1. DSP Structures for VLSI
2. Digital Systems (UG)	2. FPGA based system design
3. Analog Integrated Circuits (UG)	3. Application Specific Integrated Circuits
4. Satellite Communication(UG)	4. Advanced Computer Networks
5. Computer Networks (UG)	5. Detection & estimation
6. Microprocessors (UG)	6. Electronic packaging
7. Network theory (UG)	7. Analog IC design

(iii) Projects guided at Postgraduate level

About 5 projects are guided each year during the last 20 years

(iv) Other contribution(s)

Videos of the lectures delivered for the subjects VLSI systems and Analog Integrated circuits are recorded and put in the intranet for use by the students

14. Details of Major R&D Projects

Title of Project	Funding Agency	Duration		Status
		From	To	Ongoing/ Completed
Telematics Laboratory	AICTE, New Delhi	1995	1997	Completed
Digital library	AICTE, New Delhi	1998	2000	Completed
Setting up VLSI laboratory	MHRD, New Delhi	2000	2002	Completed
Design & Analysis of FPGA based wavepipelined structures for DSP	Ministry of Information Technology, New Delhi	2001	2003	Completed

**National Institute of Technology, Tiruchirappalli:**  
**CV of Dr. B. Venkataramani/Professor, ECE**

applications				
Design of FPGA based polyphase coded waveform generator	LRDE, Ministry of Defence, Bangalore	2003	2004	Completed
SOC based target recognition system	DST, New Delhi	2005	2007	Completed
Optimization techniques for the FPGA implementation of software defined Radio	DST, New Delhi	2006	2009	Completed
Development of signal processing systems for core temperature measurement	IGCAR, Kalpakkam	2009	2011	Completed
Embedded system development using Intel atom 56XX processor	Intel, Bangalore	2011	2012	Completed
Special Manpower Development programme for VLSI (SMDP-II)	Dept of Electronics & IT (Deity), New Delhi	2006	2011	Completed
Design and implementation of Low power analog front end modules for wireless sensor networks	Deity, New Delhi	2012	2015	Completed
Design & implementation of baseband modules for wireless sensor networks	Broadcomm Foundation, USA	2015	2017	Ongoing
C2SD/ SMDP-III	Deity, New Delhi	2015	2020	Ongoing
Design and	Deity, New Delhi	2008	2011	Completed

**National Institute of Technology, Tiruchirappalli:**  
**CV of Dr. B. Venkataramani/Professor, ECE**

Implementation of MB-OFDM UWB Transceiver Modules using Asynchronous Pipelining				
Low complexity Energy efficient Transceivers for Cognitive Radio System	UKEIRI	2012	2014	Completed
Setting up Wireless System Design lab.	FIST, DST	2012	2017	Ongoing

15. Number of PhDs guided

Name of the PhD Scholar	Title of PhD Thesis	Role(Supervisor/ Co-Supervisor)	Year of Award
G.Lakshminarayanan	Design and Analysis of FPGA based wavepipelined and pipelined structures for digital signal processing applications	Supervisor	2005
G.Seetharaman	Design & Analysis of Automation techniques for the Implementation of Wave-pipelined circuits on FPGA	Supervisor	2007
V.Amudha	Study and Evaluation of different Architectures for System on Chip Implementation of Isolated Digit Recognition System	Supervisor	2008
S.Ramasamy	Design and analysis of low power programmable OTA-C filters	Supervisor	2009
B.Malarkodi	Performance analysis of Adhoc networks	Supervisor	2011
J.Manikandan	SVM based speech recognition system	Supervisor	2012
M.Bhaskar	High speed interconnects	Supervisor	2015
S.Kumaravel	VLSI Implementation of data converters	Supervisor	2015
R. Raja	Low power Architectures for LNAs and Mixers	Supervisor	Ongoing
R. Sanjay	VLSI architectures for Frequency synthesizers	Supervisor	Ongoing
R. Greeshma	Low power Architectures for ADC / DAC	Supervisor	Ongoing
R.K. Kavitha	Design of high speed asynchronous circuits	Supervisor	Ongoing
R. Thilagavathy	Optimisation techniques for biomedical ICs	Supervisor	Ongoing
Hari Kishore	Testability for RF Front-end Modules	Supervisor	Ongoing
Senthil Rajan	Design of Low power VLSI circuits using Fuzzy logic and game theory	Supervisor	Ongoing

**National Institute of Technology, Tiruchirappalli:**  
**CV of Dr. B. Venkataramani/Professor, ECE**

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16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role)

**Conferences attended**

<i>Sl. No.</i>	<i>Name of the organizer</i>	<i>Type of conference</i>	<b>Place</b>	<i>Duration</i>
1	International Teletraffic Congress	International	Bangalore	15-19 Nov 1993
2	I.I.T. Bombay	National (NCC-96)	Bombay	16-19 Feb 1996
3	I.I.T. Madras	National (NCC-97)	Madras	Jan 31- Feb 2 '97
4	IEEE Region 10, Malaysia Chapter	International	Kualalumpur, Malaysia	Sep 24-27, 2000
5	Thiagarajar College of Engg. Madurai	National	Madurai	14-16 Feb 2002
6	P.S.G. College of Technology, Coimbatore	National	Coimbatore	21-22 Feb 2003
7	IEEE Region 10, Bangalore Chapter	International	Bangalore	15-17 Oct 2003
8	Intel	Asia Academic forum 2007	Kualalumpur, Malaysia	Nov 10-12, 2006
9	IEEE	International	Singapore	Nov 11-15, 2014
9	Intel	Asia Academic forum 2015	New Delhi	Dec 2015
10	IEEE	International	Bangalore	Dec 2015

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convenor / Co-Convenor)

Title of Activity	Level of Event (International/ National/ Local)	Date (s)	Role	Venue

18. Invited Talks delivered

Topic	Date	Inviting Organization

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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19. Membership of Learned Societies

Type of Membership (Ordinary Member/ Honorary Member / Life Member )	Organization	Membership No. with date
Life Member	IETE	F169675
Member	IEEE	93237014 2015

20. Academic Foreign Visits

Country	Duration of Visit	Programme
USA	June 1- 28, 2010	Visit to California State University , Northridge
USA	March 15-22, 2011	Interaction with US universities
USA	April 1-14, 2014	Visit to Georgia University , USA
Malaysia	Nov 11-14, 2000	Presentation of paper in Conference
Malaysia	Nov 10-12, 2006	Intel Asia Academic forum
Singapore	Nov 11-15, 2014	Presentation of paper in Conference



National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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21. Publications

(A) Refereed Research Journals:

Author(s)	Title of Paper	Journal	Volume (No.)	Page numbers	Year	Impact Factor of the Journal (Optional)
R. Raja, Ramesh Theegala, and B. Venkataramani	A class-E power amplifier with high efficiency and high power-gain for wireless sensor network	Springer - Microsystem Technologies	2		July 2016	
S. Kumaravel, Anand Kukde, B. Venkataramani, R. Raja	A high linearity and high gain Folded Cascode LNA for narrowband receiver applications	Microelectronics Journal	54	101-108	August 2016	
S. Kumaravel and B. Venkataramani	A Current Steering Positive Feedback Improved Recycling Folded Cascode OTA	World Academy of Science, Engineering and Technology (WASET), International Journal of Electrical, Electronic Science and Engineering	8	544-551	544-551 April 2014	
Bhaskar. M, Srinivas	Dynamic Self	WSEAS	13	117- 128	2014	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

Gantasala, and Venkataramani	controllable Surfing for Differential on-chip wavepipelined serial interconnect	Transactions on Circuits and Systems				
Bhaskar. M and Venkataramani. B	Differential voltage mode transceiver for on-chip global interconnects	Journal of Low Power Electronics, American Scientific Publishers	10		June 2014	
Bhaskar. M, Srinivas Gantasala and Venkataramai. B	Bidirectional differential on-chip wave-pipelined serial inteconnect with surfing	Microsystems Technologies, Springer			2015	
S. Kumaravel, K. N. Bharadwaj Tirumala, B. Venkataramani, and R. Raja	A Power Efficient Low Noise Preamplifier for Biomedical Applications	Journal of Low Power Electronics	9	501-509	Dec 2013	
M. Bhaskar , A. Jaswanth, B. Venkataramani	Design of a novel differential on-chip wave-pipelined serial interconnect with surfing	Journal of Microprocessors and Microsystems, Elsevier	37	649–660	August–October 2013	
Bhaskar. M and Venkataramani. B	Transceiver for Differential Wave Pipe-Lined Serial Interconnect with Surfing	International Journal of Electrical, Electronic Science and Engineering	8	155-162	March 2013	
J.Manikandan and	System-on-	Springer	4	347-363	August 2013	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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B.Venkataramani	programmable-chip implementation of diminishing learning based pattern recognition system	International Journal of Machine Learning and Cybernetics				
Manikandan, J. and B.Venkataramani	Evaluation of Multi-class SVM Classifiers using Optimum threshold based Pruning Technique	IET Signal Processing	5	506-513	August 2011	
S. Ramasamy , B. Venkataramani	A Low Power Reconfigurable Analog Baseband Block for Software Defined Radio	Journal of signal processing system, Springer, USA	6	131-144	2011	
S. Ramasamy , B. Venkataramani	A Low Power Reconfigurable Analog Baseband Block for Software Defined Radio	Journal of signal processing system, Springer, USA	6	131-144	2011	
Manikandan, J. and B.Venkataramani	Design of a Real Time Automatic Speech Recognition System using modified one against all SVM Classifier	Elsevier Microprocessors and Microsystems	35	568-578	Aug 2011	
J. Manikandan, B. Venkataramani	Study and Evaluation of a	Elsevier journal on	73	10-12	June 2010	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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	Multi-class SVM Classifier using Diminishing Learning Technique	Neurocomputing				
B.Malarkodi, B.Prasana and B.Venkataramani	A Battery Power Scheduling Policy with Hardware Support In Mobile Devices	International journal on applications of graph theory in wireless ad hoc networks and sensor networks	2		September 2010	
B. Malarkodi, S. K. Riyaz Hussain, and B. Venkataramani	Venkataramani, "Performance Evaluation of AOMDV-PAMAC Protocols for Ad Hoc Networks	WSAET	62	539-542	Feb 2010	
B.Malarkodi, B.Venkataramani	Protocols for increasing the lifetime of nodes of ad hoc wireless networks	International Journal on communication technology" IJCT.Volume	1	7-16	June 2009	
G. Seetharaman, B.Venkataramani	Automation Schemes for FPGA Implementation of Wave-Pipelined Circuits	ACM Transactions on Reconfigurable Technology and Systems	2	1-19	June 2009	
V Amudha and B. Venkataramani	System on programmable chip implementation of neural network-based isolated digit	International Journal of Electronics	96	153-163	Feb 2009	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

	recognition system					
S. Ramasamy, B. Venkataramani* and P. Meenatchisundaram	A low power CMOS voltage reference circuit with sub threshold MOSFETs	Int. J. Information and Communication Technology	2	94-107	2009	
V. Amudha, B.Venkataramani, R. Vinoth kumar and S. Ravishankar	Software/Hardware Co-Design of HMM Based Isolated Digit Recognition System	Journal Of Computers	4	154-159	February 2009	
G. Seetharaman, B.Venkataramani and G.Lakshminarayanan	1. Design and FPGA implementation of self-tuned wave pipeline filters with Distributed Arithmetic 2008	AlgorithmCircuits Syst Signal Process, Birkhäuser Boston		261-276	2008	
G. Seetharaman, B. Venkataramani and G. Lakshminarayanan	Automation techniques for implementation of hybrid wave-pipelined 2D DWT	Journal on Real time image processing, Springer Verlag ,USA	3	217-229	2008	
G. Seetharaman, B. Venkataramani and G. Lakshminarayanan	Hybrid wave-pipelined 2D DWT using lifting Scheme,"	VLSI design, Hindawii journal		18	2008	
G.Seetharaman, B.Venkataramani and	Design and FPGA implementation of	Transaction of IETE journal of	52	281-286	July-August 2006	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

G.Lakshminarayanan,	self tuned wave pipeline filters	research				
B.Malarkodi, B.Venkataramani and X.T. Pradeep	Performance evaluation of AODV protocol with black list table for prevention of Denial of service attacks in wireless Ad hoc networks	WSEAS Transactions on Communications	5	107-114	January 2006	
V. Amudha, B. Venkataramani and G.Seetharaman	Design and system on chip implementation of image encoders	WSEAS transactions on Circuits & Systems	4	1292-1299	October 2005	
G. Seetharaman, B. Venkataramani and G. Lakshminarayanan	Design and FPGA implementation of wave pipelined lifting scheme for two level 2D-DWT	WSEAS transactions on Circuits & Systems	4	1284-1291	October 2005	
G. Lakshminarayanan, B. Venkataramani	Optimization techniques for FPGA based wave-pipelined DSP blocks	IEEE Transactions on Very Large Scale Integration (VLSI) Systems	13	783-793	July 2005	
B. Venkataramani, Sanjay K. Bose, K.R. Srivathsan	Queueing analysis of a non-preemptive MMPP/D/1 priority system	Computer Communications	20	999-1018	1997	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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B) Conferences/Workshops/Symposia Proceedings

Author(s)	Title of Abstract/ Paper	Title of the Proceedings	Page numbers	Conference Theme	Venue	Year
R.Raja, Anand A. kukde, and B.Venkataramani	Design of Low Power Receiver Front-end for IEEE 802.15.14 Wireless Standard	4th International Conference on Computing, Communication and Sensor Network (CCSN2015),	10-15	Computing, Communication and Sensor Network		December 2015
R.Raja, Ramesh Theegala, B.Venkataramani	Design of Two-Stage Class-E Power Amplifier for ISM- Band Applications	2nd International Conference on Microelectronics, Circuits and Systems (Micro2015)	10-15	Microelectronics, Circuits and Systems		July 2015
R.Raja, Ramesh Theegala, B.Venkataramani	Design of Fully Differential Low- Power Merged LNA- Mixer for WSNs	2nd International Conference on Microelectronics, Circuits and Systems (Micro2015)	25-30	Microelectronics, Circuits and Systems		July 2015
Malathi. D, Greeshma. R, Sanjay. R, Venkataramani. B	A 4 bit medium speed flash ADC using inverter based comparator in 0.18 $\mu$ m CMOS	In Proceedings of 19th IEEE International Symposium on VLSI Design and Test (VDATE)	15	International Symposium on VLSI Design and Test		June, 2015
Malathi. D, Sanjay. R, Greeshma. R,	A 4 bit low power process tolerant flash ADC in 0.18 $\mu$ m	3rd IEEE International Conference on	1-5	IEEE International Conference on Signal Processing, Communication and Networking (ICSCN)		March 2015



National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

Venkataramani. B	CMOS	Signal Processing, Communication and Networking (ICSCN)				
Kalra. P, Kukde. A, Venkataramani. B	CORDIC based BPSK modulator	Proceedings of IEEE International Conference on Computer and Communication Technology (ICCCT)	335-339	Computer and Communication Technology		Sep. 2014
Kalra, P, Vemishetty N, Venkatramani, B	CORDIC based Universal Modulator	Recent Advances in Engineering and Computational Sciences (RAECS-2014)	1,5,6-8	Advances in Engineering and Computational Sciences		March 2014
Bhaskar.M, Srinivas Gantasala and Venkataramani.B	Dynamic Self controllable Surfing for Differential on-chip wave-pipelined serial interconnect	1st International conference on Microelectronics, Circuits and Systems (MICRO-2014)		Microelectronics, Circuits and Systems		July 2014
Kukde. A. A, Kumaravel. S, Venkataramani. B	A low power folded cascade low noise amplifier for multi standard wireless applications	In Proceedings of IEEE International Conference on Computer and Communication Technology (ICCCT)	193-198	International Conference on Computer and Communication Technology		Sep. 2014
Kukde. A. A, Kumaravel. S, Venkataramani. B	A high linearity folded cascode Low Noise Amplifier for wireless receivers	A high linearity folded cascode Low Noise Amplifier for	1344-1348	International Conference on Circuit, Power and Computing Technologies		March, 2014

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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		wireless receivers In Proceedings of IEEE International Conference on Circuit, Power and Computing Technologies (ICCPCT)				
J. Manikandan, V.K.Agrawal and B.Venkataramani	Design of a Biometric Security System using Support Vector Machine Classifier	Int. Springer Conf. on Advanced Computing, Networking and Informatics	12-14	Conf. on Advanced Computing, Networking and Informatics	Raipur	June 2013
Naresh V., B.Venkataramani , Abhishek K and J.Manikandan	PSoC based Isolated Speech Recognition System	IEEE Int. Conf. on Communication and Signal Processing, ICCSP 13	693 - 697	Communication and Signal Processing		April 2013
J.Manikandan and B.Venkataramani	Hardware implementation of Voice operated robot using Support Vector Machine Classifier	IEEE Int. Conf. on Advanced Computing	13-15	Advanced Computing	Chennai	Dec 2012
Bhaskar.M, Prasannakumar. D and Venkataramani.B	Design of Differential voltage mode Transmitter for On- chip serial link based on Method of Logical Effort	IEEE-ICCCNT			Coimbatore	July 2012

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

Bhaskar, M.; Parthiban, D.; Venkataramani, B	Design and implementation of surfing scheme to wave pipelined differential serial interconnect	Proceedings of IEEE conference RAICS 2011	232 – 235	Advances in intelligent communication systems		2011
Bhaskar, M.; Sridevi, D.; Venkataramani, B	A low power, low latency tunable Quasi-resonant interconnect using active inductor	Proceedings of IEEE conference RAICS 2011	295 - 298	Advances in intelligent communication systems		2011
Karutharaja, V; Bhaskar, M.; Venkataramani, B	Synchronization of on-chip serial interconnect transceivers using Delay Locked Loop (DLL)	Proceedings of IEEE conference ICSCCN	213 - 216	Signal Processing, Communication, Computing and Networking		2011
S.Kumaravel, B.Venkataramani and Aryam Gupta	VLSI Implementation of Gm-C filter using Modified Nauta OTA with double CMOS pair	Proceedings of IEEE conference RAICS 2011	216 - 220	Advances in intelligent communication systems		2011
J. Manikandan, B. Venkataramani, K. Girish, H. Karthic, V. Siddharth	Hardware Implementation of Real-Time Speech Recognition System Using TMS320C6713 DSP	24th International Conference on VLSI Design	250-255	VLSI Design		January, 2011
B.Malarkodi, SK.Riyas Hussain, B.Venkataramani	Performance evaluation of AOMDV-PAMAC protocols for adhoc networks	International Conference on Computer, Electrical, and Systems Science	1201-1204	Computer, Electrical, and Systems Science and Engineering		Feb 2010

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

		and Engineering ICCESSE 2010				
B.Malarkodi, S.Bavadharini, B.Venkataramani	Power Aware MAC protocol for wireless Adhoc networks	IEEE sponsored International conference on recent advancements in electrical sciences,ICRAES 2010	220-224	recent advancements in electrical sciences		
Malarkodi, B.; Gopal, P.; Venkataramani, B	Performance Evaluation of Adhoc Networks with Different Multicast Routing Protocols and Mobility Models	Proc. Of International Conference on Advances in Recent Technologies in Communication and Computing ,ICRAES 2010	81 - 84	Recent Technologies in Communication and Computing		
Malarkodi, B.; Gopal, P.; Venkataramani, B.	Performance Evaluation of Adhoc Networks with Different Multicast Routing Protocols and Mobility Models	Proc. Of International Conference on Advances in Recent Technologies in Communication and Computing, 2009	81-84	Recent Technologies in Communication and Computing		
B.Malarkodi, B.Prasanna, B.Venkataramni	A scheduling policy for battery management in mobile devices	NETCOM IEEE International Conference December 27 2009	83-88	NETCOM	Chennai	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

S Ramasamy B Venkataramani, Venkata Subba reddy	A low power tuning scheme for low frequency Continuous time filters	IEEE Region 10 conference TENCN 2009 Nov 2009	23-26	TENCN		
Sanjay Talekar, S Ramasamy, G Lakshminarayanan, B Venkataramani	A low power 700MSPS 4bit time interleaved SAR ADC in 0.18um CMOS	”, IEEE Region 10 conference TENCN2009	23-26	TENCN		
Manikandan J, B Venkataramani, P Preethi, G Sananda, K V Sadhana	Implementation of a Phoneme Recognition System using Zero-Crossing and Magnitude Sum Function	IEEE Region 10 conference TENCN2009	23-26	TENCN		
Manikandan, J.; Venkataramani, B	Design of a modified one-against-all SVM classifier	IEEE International Conference on Systems, Man and Cybernetics	1869 - 1874			
Malarkodi, B.; Rakesh, P.; Venkataramani, B	Performance Evaluation of On-Demand Multipath Distance Vector Routing Protocol under Different Traffic Models	International Conference on Advances in Recent Technologies in Communication and Computing”, International Conference on Advances in Recent Technologies in Communication	77 – 80	Recent Technologies in Communication and Computing		

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

		and Computing, 2009. ARTCom '09. 27-28 Oct. 2009				
Malarkodi, B.; Gopal, P.; Venkataramani, B	Performance Evaluation of Adhoc Networks with Different Multicast Routing Protocols and Mobility Models	International Conference on Advances in Recent Technologies in Communication and Computing, 2009. ARTCom '09. 27-28 Oct. 2009	81-84	Recent Technologies in Communication and Computing		
Talekar, S.G.; Ramasamy, S.; Lakshminarayan, G.; Venkataramani, B	500MS/s 4-b time interleaved SAR ADC using novel DAC architecture	Quality Electronic Design, 2009. ASQED 2009. 1st Asia Symposium on 15-16 July 2009		Quality Electronic Design		
Kirankumar, M.Bhaskar, R.Thilagavathy and B.Venkataramani	A Novel Low Power Multilevel Current Mode Interconnect System Ineffective to Supply voltage variations	International Conference on Optoelectronics and Communication Technology ICOICT2009  February 2009		Optoelectronics and Communication Technology	Trivandrum	
Venkateswaralu, M.Bhaskar and B.Venkataramani	Quasi-resonant interconnects: Programmable data rate implementation	International Conference on Optoelectronics and		Optoelectronics and Communication Technology	Trivandrum	

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

	using active inductor	Communication Technology ICOICT2009  26-27 February 2009				
Ramasamy, S.; Venkataramani, B.; Niranjini, R.; Suganya, K	100KHz-20MHz Programmable Subthreshold G <sub>m</sub> -C Low-Pass Filter in 0.18 $\mu$ -m CMOS,	22nd International Conference on VLSI Design, 2009, 5-9 Jan. 2009	105 – 110	VLSI Design		
Ramasamy, S.; Venkataramani, B.; Meenatchisundaram, P	A low power CMOS voltage reference circuit with subthreshold MOSFETs	International Conference on Electronic Design, 2008. ICED 2008, 1-3 Dec. 2008	1-6	Electronic Design		
Ramasamy, S.; Venkataramani, B.; Meenatchisundaram, P	A low power programmable band gap reference circuit with subthreshold MOSFETs	IEEE Region 10 Conference TENCON 2008, 19-21 Nov. 2008	1 - 6	TENCON		
Ramasamy, S.; Venkataramani, B.; Stalin, S.M.; Venkatachalam	K.Tunable band pass G <sub>m</sub> -C filter with switched transconductance cells	IEEE Region 10 Conference TENCON 2008, 19-21 Nov. 2008	1-5	TENCON		
Manikandan, J.; Venkataramani, B	Diminishing learning based SVM classifier with non-linear kernels	International Conference on Electronic Design 2008. ICED	1-6	Electronic Design		

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

		2008. 1-3 Dec. 2008				
Amudha, V.; Venkataramani, B.; Manikandan, J	FPGA implementation of isolated digit recognition system using modified back propagation algorithm	International Conference on Electronic Design, 2008. ICED 2008. 1-3 Dec. 2008	1-6	Electronic Design		
Manikandan, J.; Venkataramani, B.; Avanthi, V	FPGA Implementation of Support Vector Machine Based Isolated Digit Recognition System	22nd International Conference on VLSI Design, 2009, 5-9 Jan. 2009	347-352	VLSI Design		
Manikandan, J.; Venkataramani, B.; Amudha, V.; Arafat, A.Majed; Sahu, Hruday	A novel technique for Support Vector Machine based multi- class classifier	IEEE Region 10 Conference TENCON 2008 19-21 Nov. 2008	1-6	TENCON		
Anusha, G.; Venkateshwarlu, P.; Murugeswari, P.; Bhaskar, M.; Venkataramani, B.	An input multiplexed current mode transmitter for on-chip global interconnects,	IEEE Region 10 Conference TENCON 2008 19-21 Nov. 2008	1-5	TENCON		
Murugeswari, P.; Anusha, G.; Venkateshwarlu, P.; Bhaskar, M.; Venkataramani, B	A wide band voltage mode sense amplifier receiver for high speed interconnects	IEEE Region 10 Conference TENCON 2008, 19-21 Nov. 2008	1-5	TENCON		



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Vireen, V.; Seetharaman, G.; Venkataramani, B	Synthesis techniques for implementation of wave-pipelined circuits in ASICs	International Conference on Electronic Design, 2008	1 – 6	Electronic Design		
Venugopalachar y, N.; Vireen, V.; Seetharaman, G.; Venkataramani	BASIC implementation of self tuned wave-pipelined circuits	International Conference on Electronic Design, 2008	1 – 6	Electronic Design		
Vireen, V.; Venugopalachar y, N.; Seetharaman, G.; Venkataramani. B	Built in Self Test Based Design of Wave-Pipelined Circuits in ASICs	22nd International Conference on VLSI Design	473 – 478	VLSI Design		
J. Manikandan, B. Venkataramani and M. Jayachandran	Evaluation of Edge Detection Techniques towards Implementation of Automatic Target Recognition	International Conference on Computational Intelligence and Multimedia Applications (ICCIMA 2007)	441-445	Computational Intelligence and Multimedia Applications		
S. Ramasamy, B. Venkataramani, K. Anbugeetha	VLSI Implementation of a Digitally Tunable Gm-C Filter with Double CMOS Pair	IEEE international conference on VLSI Design, 2008	317-322	VLSI Design		
G. Seetharaman, B. Venkataramani	SOC implementation of wave-pipelined circuits	IEEE international conference on Field Programmable Techology 2007	9-16	Field Programmable Techology		

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V.Amudha, B.Venkataramani ,R.Vinoth kumar and S. Ravishankar	SOC implementation of HMM based speaker independent isolated digit recognition	IEEE international conference on VLSI Design		VLSI Design		
V. Amudha , B. Venkataramani and G. Seetharaman	Optimisation techniques for the system on chip implementation of JPEG encoder	5th WSEAS Int. Conf. on Signal Processing, Computational Geometry & Artificial Vision, Malta, 2005	94-101	Signal Processing, Computational Geometry & Artificial Vision		
G. Seetharaman, B. Venkataramani and G. Lakshminarayan an	Design and FPGA implementation of lifting scheme for 2D- DWT using wavepipelining	WSEAS Int. Conf. on Signal Processing, Computational Geometry & Artificial Vision, Malta, September 15-17, 2005	53-60	Signal Processing, Computational Geometry & Artificial Vision		
B. Malarkodi, B. Venkataramani and X.T. Pradeep	Modified AODV protocol for prevention of Denial of service attacks in wireless Ad hoc networks	5th WSEAS Int. Conf. on Applied informatics and communications, Malta, September 15-17, 2005	77-84	Signal Processing, Computational Geometry & Artificial Vision		
G. Seetharaman, B.Venkataramani , V. Amudha, Anurag	System on chip implementation of 2D DWT using lifting scheme	International Asia and South Pacific Conference on Embedded SOCs		Embedded SOC		

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G.Lakshminarayan, B.Venkataramani, M.Sasitharan, K.P.Senthil Kumar	Design and implementation of FPGA based wavepipelined multiplier accumulators	International Conf. on Circuits, Control, Communication and Devices ICCCD 2000, IIT, Kharagpur, Dec 2000	265-268	Circuits, Control, Communication and Devices		
G.Lakshminarayan, Bobby George, B. Venkataramani, A.Ramakalyan	Neural Network Controlled Shift Register Traffic Shaper for ATM Networks	IEEE TENCON '98, December 1998	33-36	TENCON		
B. Venkataramani, S.K. Bose, K.R. Srivathsan	An exact model for the queuing analysis of MMPP/D/1 queue with non-preemptive priority for applications in ATM networks,	Proc. ICCS-94, Singapore, 1994	104-108			

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B. Venkataramani, S.K. Bose, K.R. Srivathsan	Queue length density and busy period distribution of MMPP/D/1 queue with non preemptive priority for use in ATM networks	ITC Seminar, Bangalore, India. 1993	121-128			
S.Kumaravel, B.Venkataramani, Ajit Randhir, and Ramakrishna Chowtri	A Novel Fully Differential Folded Cascode Operational Transconductance Amplifier,	V DAT July 7-9 2011				
S.Kumaravel, B.Venkataramani and Akila M	Behavioural Analysis of Clock Jitter Effects in Continuous Time Sigma Delta Modulator	V DAT July 7-9, 2011				
S.Kumaravel, B.Venkataramani and Aryam Gupta	VLSI Implementation of Gm-C filter using Modified Nauta OTA with double CMOS pair	IEEE RAICS Sep 22-24, 2011, Trivandrum				
N. Sreekanth Babu, S. Ramasamy, B.Venkataramani	Design of high performance current steering DAC using pattern search algorithm	VLSI design and test symposium V DAT 2007, Aug 2007, Calcutta, India	120-129			
S. Ramasamy, B.Venkataramani, N. Sreekanth Babu	Design and implementation of 14 bit 200Msps current steering DAC using Gm/Id method	VLSI design and test symposium V DAT 2007, Aug 2007, Calcutta, India	105 -113			
V. Amudha,	SOC implementation	V DAT 2006	130-138			

National Institute of Technology, Tiruchirappalli:  
CV of Dr. B. Venkataramani/Professor, ECE

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G. Seetharaman, B. Venkataramani and G.Lakshminarayanan	Design and FPGA implementation of wavepipelined distributed arithmetic based filters	VLSI Design & Test workshop VDAT04, Mysore	216-220			
G. Lakshminarayanan, B. Venkataramani, M. Yousuff Shariff, T. Rajavelu and M. Ramesh	Self tuning circuit for FPGA based wavepipelined multipliers.	VLSI Design & Test workshop VDAT04, Mysore	93-101			
J.Senthil Kumar , G.Sriram, G.Lakshminarayanan , B.Venkataramani	Design and Implementation of FPGA based Fast Multipliers with Optimum Placement & Routing Using Structure Organizer	National Conference on VLSI design & Testing, PSG College of Technology, Coimbatore, 21-22 February, 2003				
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B.Venkataramani	High Performance DSP circuits using FPGAs”, Workshop on 'DSP/FPGA technologies	CEERI Chennai, June 24-25 2002				
M.C.Sundar, A.Senthil Kumar, B.Venkataramani , M. Bhaskar	Implementation Of FPGA Based Image Processing System With Lifting Wavelet Transform	National workshop on Computer Vision, Graphics and Image Processing, WVGIP 2002, TCE, Madurai	45-50			
K.Balaji, B.Venkataramani , M.Bhaskar, G. Lakshminarayan an	Enhancing the Performance of the TI DSP systems with FPGAs	Texas Instruments DSPFEST-2001, Bangalore				
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National Institute of Technology, Tiruchirappalli:  
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B.Venkataramani, M. Bhaskar	Digital Signal Processors	Tata McGraw-Hill Education	2002	978-0-07-070256-1
Microprocessors and Peripherals	B.Venkataramani, P.Somaskandan	Tata McGraw-Hill Education	1999	0-07-463954-4