

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

Curriculum Vitae



Brief Profile:

Manikandan R R received his Ph.D. degree from Electrical Communication Engineering, Indian Institute of Science, Bangalore in 2014. His Ph.D. thesis focuses on "Low power and low spur frequency synthesizer circuit techniques for energy efficient wireless transmitters". From 2015 to 2016, he worked as a Lead Design Engineer at Cadence Designs Systems, Bangalore. From 2016 to 2017, he was a member of Kilby Labs, Texas Instruments, Bangalore and designed ultra-low power analog circuits for an IoT power management application. From 2017 to 2023, he worked as an Analog Design Engineer at Texas Instruments and designed Isolated power and data transfer circuits, and precision analog circuits. From 2023 to 2024, he worked as an Assistant Professor at International Institute of Information Technology Bangalore (IIITB), India. He is presently working as an Assistant Professor at National Institute of Technology, Tiruchirappalli (NIT-T), India.

1. Name: Manikandan R R
2. Designation: Assistant Professor
3. Office Address:
Room No. 304, Electronics and Communication Engineering (ECE) Department,
NIT-Tiruchirappalli.
4. Mobile (Optional):
5. Email (Primary): manirr@nitt.edu
6. Field(s) of Specialization: Analog/RF circuit design, Analog VLSI
7. Employment Profile

Job Title	Employer	From	To
Assistant Professor	NIT, Tiruchirappalli	June 2024	Present
Assistant Professor	IIIT Bangalore	April 2023	May 2024
Analog Design Engineer	Texas Instruments, Bangalore	July 2017	March 2023
Member of Kilby Research Labs	Texas Instruments, Bangalore	June 2016	June 2017
Lead Design Engineer	Cadence Designs Systems, Bangalore	January 2015	May 2016

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

8. Academic Qualifications (From Highest Degree to High School):

Examination	Board / University	Year	Division/ Grade	Subjects
Ph.D	Indian Institute of Science, Bnagalore	2015	First class with distinction	Microelectronics
B.E	College of Engineering, Guindy, Chennai	2009	First class with distinction	Electronics and communication Engineering (ECE)
12th	Fatima matriculation higher secondary school	2004		State Board
10th	Fatima matriculation higher secondary school	2002		Matriculation

9. Academic/Administrative Responsibilities within the University

Position	Faculty/Department/Centre/Institution	From	To

10. Academic/Administrative Responsibilities outside the University

Position	Institution	From	To

11. Awards, Associateships etc.

Year of Award	Name of the Award	Awarding Organization
2021	Best paper award	IEEE International Conference on VLSI Design, 2021
2018	Honorable Mention Award	IEEE International Conference on VLSI Design, January 2018
2006	Institute Gold medal for proficiency in the subject of Engineering Graphics	College of Engineering, Guindy, Chennai, 2006

12. Fellowships

Year of Award	Name of the Fellowship	Awarding Organization	From (Month/Year)	To (Month/Year)

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

13. Details of Academic Work

(i) Curriculum Development

(ii) Courses taught at Postgraduate and Undergraduate levels

1. Network Analysis and Synthesis (July-November, 2024, at NIT Tiruchirappalli)
2. Analog Power Integrated Circuit (IC) Design (Jan-April term, 2024, at IITB)
3. Analog Circuits Theory (January-April term, 2024, at IITB)
4. Analog CMOS VLSI Design (August-November term, 2023, at IITB)
5. Introduction to Integrated Circuit (IC) design (August-November term, 2022, at Indian Institute of Science (IISc), Bangalore)
6. IoT Sensor node power management unit (Value added course, January-April term, 2022, at College of Engineering, Guindy, Chennai)

(iii) Projects guided at Postgraduate level

1. M. Tech Project/Thesis “Low Power, High Precision, CMOS Voltage Reference Circuit using the ZTC point of MOSFET”, Shravan Sridhar, IISc.

(iv) Other contribution(s)

14. Details of Major R&D Projects

Title of Project	Funding Agency	Duration		Status
		From	To	Ongoing/ Completed

15. Number of PhDs guided

Name of the PhD Scholar	Title of PhD Thesis	Role(Supervisor/ Co-Supervisor)	Year of Award

16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role)

Date (s)	Title of Activity	Level of Event	Role (Participant/ Speaker/ Chairperson,	Event Organized by	Venue

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

		(International/ National/ Local)	Paper presenter, Any other)		

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convenor / Co-Convenor)

Title of Activity	Level of Event (International/ National/ Local)	Date (s)	Role	Venue

18. Invited Talks delivered

1. "Performance specific, technology look up table based design methodology for LDOs", Tutorial delivered at 28th IEEE International Symposium on VLSI Design and Test (VDAT-2024), India, and at IEEE VLSI Chapter, IISc, Bangalore.
2. "Isolated Power and Data Transfer Circuits", Invited talk at IEEE SSCS/Photonics Society Joint PES Institute of Technology Bangalore Student Chapter, on 22nd November, 2023.
3. "Cryo-CMOS Circuits and Systems for Quantum Computing Applications", Samvaad series Talk at IIIT-B, on 11th September, 2023.
4. "Ultra low power voltage reference circuits", Workshop series on Advanced communication systems at IIIT-B, on 24th June, 2023.

19. Membership of Learned Societies

Type of Membership (Ordinary Member/ Honorary Member / Life Member)	Organization	Membership No. with date

20. Academic Foreign Visits

**National Institute of Technology, Tiruchirappalli:
Performa for CV of Faculty/ Staff Members**

Country	Duration of Visit	Programme

21. Publications

(A) Refereed Research Journals:

J1. "A zero charge-pump mismatch current tracking loop for reference spur reduction in PLLs", Manikandan R R, Bharadwaj Amrutur, Microelectronics journal, Elsevier, June 2015.

J2. "A digital frequency multiplication technique for energy efficient transmitters", Manikandan R R, Abhishek Kumar, Bharadwaj Amrutur, IEEE Transactions on Very Large Scale Integration (TVLSI) systems, March 2014.

J3. "Experimental study on substrate noise effects of a pulsed clocking scheme on PLL performance", Manikandan R R, Bharadwaj Amrutur, IEEE Transactions on Circuits and Systems II: Express Briefs, December 2013.

(B) Conferences/Workshops/Symposia Proceedings

C1. "Overview of Cryo-CMOS Devices and Circuits for Quantum Computing Applications", Manikandan R R, International Symposium on Smart Electronic Systems (IEEE – iSES), Ahmedabad, 2023 (Invited paper).

C2. "150nA Iq, Quad Input - Quad Output, Intelligent Integrated Power Management for IoT Applications", Vipul Singhal, Rajat Chauhan, Vinod Menezes, Manikandan R R, Raveesh Magod, Mahesh Mehendale, Anantha Chandrakasan, International Conference on VLSI Design, 2021 (Best Paper Award).

C3. "A 1.2 pJ/cycle KHz Timer Circuit for Heavily Duty-Cycled Systems", Manikandan R R, Vipul Singhal, Rajat Chauhan, Vinod Menezes, Mahesh Mehendale, International Conference on VLSI Design, January 2018 (Honorable Mention Award).

C4. "A High Performance Switchable Multi-band Inductor Structure for LC-VCOs", Manikandan R R, Venkata Narayana Rao Vanukuru, International Conference on VLSI Design, January 2017.

C5. "A Parameterized Cell Design for High-Q, Variable Width and Spacing Spiral Inductors", Manikandan R R, Venkata Narayana Rao Vanukuru, Anjan Chakravorty, Bharadwaj Amrutur, International Microwave and RF Conference (IMaRC), December 2014.

C6. "Design and modeling of high-Q variable width and spacing, planar and 3-D stacked spiral inductors", Manikandan R R, Venkata Narayana Rao Vanukuru, Anjan Chakravorty, Bharadwaj Amrutur, International symposium on VLSI Design and Test (VDAT), July 2014.

National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

(C) Patents granted

P1. "Self Calibrating ON-OFF Keying based Digital Isolator", Patent publication.No. US20230025757A1, R. R. Manikandan, Anurag kumar Shrivastava, Anant Kamath, et. al., January 2023.

P2. "Single inductor multiple output regulator", Patent publication.No. US11190105B1, Vipul Kumar Singhal, R. R. Manikandan, Rajat Chauhan, Vinod Joseph Menezes, November 2021.

P3. "Load current measurement", Patent publication.No. US10855184B2, Vinod Joseph Menezes, R. R. Manikandan, Rajat Chauhan, Vipul Kumar Singhal, Mahesh Madhukar Mehendale, Kaichien Tsai, December 2020.

P4. "Ultra-low energy per cycle oscillator topology", Patent publication.No. US2019/0028089-A1, R. R. Manikandan, January 2019.

(C) Books & Monographs

Author(s)	Title of Book/Monograph	Name of Publishers	Year of Publication	ISSN/ISBN Number