



## National Institute of Technology, Tiruchirappalli: Performa for CV of Faculty/ Staff Members

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### 8. Academic Qualifications (From Highest Degree to High School):

Examination	Board / University	Year	Division/ Grade	Subjects
Ph.D	Indian Institute of Technology Patna	2023	NA	Electrical Engineering
M.Tech	National Institute of Technology Durgapur	2014	First	(Microelectronics and VLSI) Electronics and Communication Engineering
B.Tech	Pragati Engineering College (Affiliated to JNTUK)	2012	First	Electronics and Communication Engineering

### 9. Academic/Administrative Responsibilities within the University

Position	Faculty/Department/Centre/Institution	From	To

### 10. Academic/Administrative Responsibilities outside the University

Position	Institution	From	To

### 11. Awards, Associateships etc.

Year of Award	Name of the Award	Awarding Organization

### 12. Fellowships

Year of Award	Name of the Fellowship	Awarding Organization	From (Month/Year)	To (Month/Year)
2012-2014	AICTE Post Graduate (PG) Scholarship Scheme	Ministry of Education (formerly MHRD), Government of India	Aug-2012	May-2014
2018-2022	Institutional fellowship by IIT Patna	Ministry of Education (formerly	Jan -2018	Dec-2022

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		MHRD), Government of India		

13. Details of Academic Work

- (i) Curriculum Development
- (ii) Courses taught at Postgraduate and Undergraduate levels  
VLSI System, Professional Ethics.
- (iii) Projects guided at Postgraduate level
- (iv) Other contribution(s)

14. Details of Major R&D Projects

Title of Project	Funding Agency	Duration		Status
		From	To	Ongoing/ Completed

15. Number of PhDs guided

Name of the PhD Scholar	Title of PhD Thesis	Role(Supervisor/ Co-Supervisor)	Year of Award

16. Participation in Workshops/ Symposia/ Conferences/ Colloquia /Seminars/ Schools etc. (mentioning the role)

Date (s)	Title of Activity	Level of Event (International/ National/ Local)	Role (Participant/ Speaker/ Chairperson, Paper presenter, Any other)	Event Organized by	Venue

17. Workshops/ Symposia/ Conferences/ Colloquia/Seminars Organized (as Chairman/ Organizing Secretary/ Convenor / Co-Convenor)

Title of Activity	Level of Event (International/ National/ Local)	Date (s)	Role	Venue

18. Invited Talks delivered

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Topic	Date	Inviting Organization

19. Membership of Learned Societies

Type of Membership (Ordinary Member/ Honorary Member / Life Member )	Organization	Membership No. with date
Member	IEEE	96181355

20. Academic Foreign Visits

Country	Duration of Visit	Programme
Sweden	Nov 2019	Conference NMDC 2019

21. Publications

(A) Refereed Research Journals:

Author(s)	Title of Paper	Journal	Volume (No.)	Page	Year	Impact Factor of the Journal (Optional)
A. Maniyar, S. Das, P.S.T.N. Srinivas, P. K. Tiwari	Geometry-Driven Thermal Noise Trends in GAA Nanowire Devices	Silicon	Early Access		2026	3.3
B. V. Rao, A. Kumar, P.S.T.N. Srinivas, B. Bhowmick	Dielectric Modulation-Based High- Sensitivity Biomolecular Detection Using Ge/Si Heterostructure ES Fin- TFET Biosensors: A Detailed Performance Study	Sensing and Imaging	27 (1)		2026	2
R. Raj, S. Moparathi, A. Kumar, P. K. Tiwari, P.S.T.N. Srinivas	Computational investigation of trapezoidal channel profiles in Gate- All-Around (GAA) FETs for digital performance	Micro and Nanostructures	211		2025	3
S. Kumar, A. Kumar, P.S.T.N. Srinivas	Investigation of BTBT-Triggered Split-Gate Junctionless Nanosheet FETs for Analog and RF Applications	Transactions on Electrical and Electronic Materials	26		2025	1.9
A. Maniyar, P. Raj, P.S.T.N. Srinivas, A. Kumar, K. S. Chang-Liao, P. K. Tiwari	Impact of Process-Induced Inclined Side-Walls on Gate Leakage Current of Nanowire GAA MOSFETs	IEEE Transactions on Electron Devices	71 (3)		2024	3.2
T. S. Kumar, A. Hazarika, P.S.T.N. Srinivas, P. K.	A machine learning approach to accelerate reliability prediction in nanowire FETs from self-heating	Microelectronics Reliability	161		2024	1.9

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Tiwari, A. Kumar	perspective					
P.S.T.N. Srinivas, N. A. Kumari, A. Kumar, P. K. Tiwari, K. G. Sravani	Impact of ambient temperature on CombFET for sub-5-nm technology nodes: An RF performance perspective	Microsystem Technologies	31 (4)		2024	1.8
S. S. Katta, T. Kumari, P.S.T.N. Srinivas, P. K. Tiwari	Logic-in-memory application of silicon nanotube-based FBFET with core-source architecture	Microelectronics Journal	146		2024	2.3
P.S.T.N. Srinivas, S. Jit, P. K. Tiwari	Impact of self-heating on thermal noise in In <sub>1-x</sub> Ga <sub>x</sub> As GAA MOSFETs	Microelectronics Journal	131		2023	2.3
A. Maniyar, P.S.T.N. Srinivas, P. K. Tiwari, K. S. Chang-Liao	Impact of process-induced inclined sidewalls on gate-induced drain leakage (GIDL) current of nanowire GAA MOSFETs	IEEE Transactions on Electron Devices	69 (9)		2022	3.2
S. Singh, P.S.T.N. Srinivas, A. Kumar, P. K. Tiwari	Physical insight into self-heating induced performance degradation in RingFET	Silicon	14 (13)		2022	3.3
P.S.T.N. Srinivas, A. Kumar, P. K. Tiwari	Effect of self-heating on small-signal parameters of In <sub>0.53</sub> Ga <sub>0.47</sub> As based gate-all-around MOSFETs	Semiconductor Science and Technology	36		2021	2.1
P.S.T.N. Srinivas, P. K. Tiwari	Impact of Self-Heating on Linearity Performance of In <sub>0.53</sub> Ga <sub>0.47</sub> As-Based Gate-All-Around MOSFETs	IEEE Transactions on Device and Materials Reliability	22 (1)		2021	2.3
V. K. Dixit, R. Gupta, P.S.T.N. Srinivas, S. Dubey	Back Bias Induced Modeling of Subthreshold Characteristics of SOI Junctionless Field Effect Transistor (JLFET)	Silicon	13 (6)		2021	3.3
P.S.T.N. Srinivas, A. Kumar, P. K. Tiwari	Threshold Voltage Modeling of tri-Gate Schottky-Barrier (TGSB) Field-Effect-Transistors (FETs)	Silicon	13		2021	3.3
V. K. Dixit, R. Gupta, V. Purwar, P.S.T.N. Srinivas	Effect of Substrate Induced Surface Potential (SISP) on Threshold Voltage of SOI Junction-Less Field Effect Transistor (JLFET)	Silicon	12 (4)		2021	3.3
D. Gola, B. Singh, P.S.T.N. Srinivas, P. K. Tiwari	Thermal noise models for trigate junctionless transistors including substrate bias effects	IEEE Transactions on Electron Devices	67 (1)		2020	3.2
P.S.T.N. Srinivas, A. Kumar, S. Jit, P. K. Tiwari	Self-heating effects and hot carrier degradation in In <sub>0.53</sub> Ga <sub>0.47</sub> As gate-all-around MOSFETs	Semiconductor Science and Technology	35		2020	2.1
A. Kumar, P.S.T.N. Srinivas, P. K. Tiwari	An insight into self-heating effects and its implications on hot carrier degradation for silicon-nanotube-based double gate-all-around (DGAA) MOSFETs	IEEE Journal of the Electron Devices Society	7		2019	2.3

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**(B) Conferences/Workshops/Symposia Proceedings**

Author(s)	Title of Abstract/ Paper	Title of the Proceedings	Page numbers	Conference Theme	Venue	Year
A. Maniyar, P.S.T.N. Srinivas, P. K. Tiwari	Impact of Process-Induced Inclined Sidewalls On Small Signal Parameters of Silicon Nanowire GAA MOSFET	TENCON 2023 - 2023 IEEE Region 10 Conference (TENCON)	1-6	Engineering Tomorrow: The Sustainability-driven Innovation for Post Outbreak Era	Le Meridien Hotel, Chiang Mai, Thailand	2023
P.S.T.N. Srinivas, A. Kumar, P. K. Tiwari	In <sub>0.53</sub> Ga <sub>0.47</sub> As Nanosheet MOSFETs with Self-Heating Effects	2022 IEEE Silchar Subsection Conference (SILCON)	1-5	Advances in Electrical, Electronics, Computer Science and Instrumentation	National Institute of Technology Silchar, Assam, India	2022
A. Kumar, P.S.T.N. Srinivas, P. K. Tiwari	Analytical Modeling of Subthreshold Current and Subthreshold Swing of Schottky-Barrier Source/Drain Double Gate-All-Around (DGAA) MOSFETs	2019 IEEE International Symposium on Smart Electronic Systems (iSES)	1-4	Smart Electronic Systems: Hardware, Software and Integration	NIT Rourkela, Odisha, India	2019
A. Kumar, P.S.T.N. Srinivas, P. K. Tiwari	Compact drain current model of silicon-nanotube based double gate-all-around (DGAA) MOSFETs incorporating short channel effects	2019 IEEE 14th Nanotechnology Materials and Devices Conference (NMDC)	1-5	Nanotechnology Materials and Devices	KTH Royal Institute of Technology, Stockholm, Sweden	2019
P.S.T.N. Srinivas, A. Kumar, P. K. Tiwari	Effects of Lateral Spreading in 2-Dimensional	2019 IEEE 9th International Nanoelectronics Conferences	1-4	Nanoelectronics for a Sustainable Future	Kuching, Sarawak, Malaysia	2019

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	Non-Uniform Doped Junctionless FinFETs	(INEC)				
A. Kumar, P.S.T.N. Srinivas, P. K. Tiwari	Physical insight into self-heating effects in ultrathin junctionless gate-all-around FETs	2019 IEEE 9th International Nanoelectronics Conferences (INEC)	1-4	Nanoelectronics for a Sustainable Future	Kuching, Sarawak, Malaysia	2019
A. Kumar, P.S.T.N. Srinivas, P. K. Tiwari	Analytical Threshold Voltage Model of Schottky-source/drain (Schottky-S/D) double gate-all-around (DGAA) Field-Effect-Transistors (FETs)	2019 Devices for Integrated Circuit (DevIC)	1-5	Solid-State Devices, Circuits and Systems	Kalyani Government Engineering College, Kalyani, West Bengal, India	2019
P.S.T.N. Srinivas, V. K. Pulluri, C. Kumar, A. K. Mal	Implementation of 32 nm FinFET voltage controlled oscillator	International Conference for Convergence of Technology (I2CT) 2014	1-5	Convergence of Technology	Pune, Maharashtra, India	2014
P. Dhilleswararao, R. Mahapatra, P.S.T.N. Srinivas	High SNM 32nm CNFET based 6T SRAM Cell design considering transistor ratio	2014 International Conference on Electronics and Communication Systems (ICECS)	1-4	Electronics and Communication Systems	Coimbatore, Tamil Nadu, India	2014

(C) Books & Monographs

Author(s)	Title of Book/Monograph	Name of Publishers	Year of Publication	ISSN/ISBN Number