Department of Electronics & Communication Engineering

National Institute of Technology, Tiruchirappalli

24 Feb 2020

ADVERTISEMENT FOR THE TEMPORARY POST OF PROJECT DESIGN ENGINEER IN ECE DEPT

Applications are invited from M.E/M.Tech graduates with specialization in VLSI and B.E/B.Tech in ECE for the temporary post of Project Design Engineer in the consultancy project on **Algorithmic approach to achieve maximum functional coverage using Constrained Random verification platform**. The selected staff would be required to work on developing algorithms for design verification.

- The applicants are expected to have a sound knowledge of design verification and exposure to Hardware Description Languages such as Verilog, VHDL and System Verilog. Minimum experience of two years in the relevant field is preferred.
- Candidates must have a GATE score.
- Salary: Rs.25,000/= per month (consolidated)
- Duration of appointment: 6 months (purely on Temporary basis)
- Contract may be terminated with a minimum one month period of notification
- Number of Vacancy: 1
- Date/ Time of **Walk-in Interview**: 06th March 2020 /11 A.M
- Venue: ECE Department Conference Hall, Silver Jubilee Block, NIT-Trichy.
- Selected candidates will be communicated only through e-mail.
- Candidates are expected to join immediately, in case if they are selected.
- No TA/DA will be provided.
- Decision of the Selection Committee is final.
- At the time of interview, applicants are expected to appear with the following documents.
    - Photo
    - Copy of resume
    - Proof for education qualification
    - Proof for experience

For any query related to this advt. send your e-mail to **ece.projects.nitt@gmail.com** with subject as: Project Design Engineer advt.

Project Coordinator,

Algorithmic approach to achieve maximum functional coverage using Constrained Random verification platform

ECE Dept.,

NIT, Trichy 620015